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Design and Development of an APD algorithm development board for Positron Emission Tomography

Rakesh Mallem
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a thesis written by Rakesh Mallem entitled "Design and Development of an APD algorithm development board for Positron Emission Tomography." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed K. Islam, Major Professor

We have read this thesis and recommend its acceptance:

Itamar Elhanany, Ethan Farquhar

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

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Design and Development of an APD algorithm development board for Positron Emission Tomography

A Thesis
Presented for the
Master of Science Degree
The University of Tennessee, Knoxville

Rakesh Mallem
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ABSTRACT

Using the PET scanner, three dimensional images of the human body with sufficient detail can be viewed which help physicians to visualize both normal metabolic functions and discover the chemical processes underlying physical abnormalities. Commercial PET scanners employ Photo Multiplier Tubes to detect the anti-matter annihilation photons and amplify the signals to a suitable level for digital sampling. Photomultiplier tubes provide extremely high sensitivity and exceptionally low noise compared to other photosensitive devices currently used to detect radiant energy in the ultraviolet, visible and near infrared regions. A combined magnetic resonance positron emission tomography (MR-PET) modality would require a solid-state photo detector due to the known gain/timing variation of PMTs with variable magnetic field. PET detector block designs have been described and implemented in the literature using APD photo detectors at moderate values of gain. The APD Algorithm Development Board is basically a signal processing board which receives the integrated APD analog signals and outputs a digital event packet composing of position and timing data for each detected photon. These digital event packets are digitally transmitted to a downstream module for comparison with opposing detectors to detect the coincidence photons fundamental to PET. The main functions are to process analog signals from the APDs to determine if an energy qualified gamma ray event has been detected, localize the crystal position and time of the event, and transmit the event information to the control interface, en route to a coincidence processor.

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1 INTRODUCTION AND OVERVIEW

1.1 Introduction

Commercial whole body Positron Emission Tomography (PET) medical scanners require the location of thousands of lines of response (LORs) to create sinograms. These sinograms compose the basic data required for the reconstruction of a physical and quantitative representation of positron activity inside the scanner field of view. PET Noise Effective Count Rate (NECR) is a measure of the scanner's signal-to-noise ratio, which is optimized when minimal timing uncertainty exists in the detection of two coincident events.

The measured coincident events contained in a particular time frame overestimate the positron activity since the total number of events includes both true coincident events, derived from β^+ (positron) emission, as well as independent and unrelated singles events. These overlapping singles events which occur in the true coincidence or prompt window produce additional events known as randoms. These randoms must be subtracted from the total measured coincident events for an accurate estimate of the imaged positron activity. However, since the mean random rate does not depend upon the absolute time position of the coincidence window, a large artificial time shift in the absolute time window position from the true window allows the mean random rate to be easily determined.

Since the number of randoms scale directly with the specified coincidence window of the gantry, it is desirable to keep the window as small as possible while detecting all true positron annihilations. The coincidence window size in practice is reduced to allow all true coincidence events to be detected while minimizing the number of randoms. The randoms contribution may be minimized at the system level by designing a detector with an optimum 1:1 crystal/photo detector coupling ratio to obtain as accurate timing as possible. The detected photoelectron yield is near ideal and electronic transit time walk and timing variance from the summation of multiple photo detectors is eliminated.

Unfortunately, since thousands of crystals are required in a whole body system to obtain a good positional resolution, some type of photo detector sharing must be used to decrease the number of photo detectors required per scanner. The cost of 1:1 coupling is still prohibitively high for a commercial whole body scanner in the current market.

Since the effective photon yield and initial photon rate from the scintillation crystal is reduced in photo detector sharing, the timing of this lower cost detector is degraded from the ideal 1:1 coupling. Since the crystal timing has been degraded, the signal processing electronics need to minimize any additional degradation caused by algorithm or analog processing. The electronic processing contribution to crystal timing resolution should be kept as low as possible and has been classically done with an analog constant fraction discriminator (CFD) and time to digital converter (TDC).

Using current analog CFD circuits, the crystal timing resolution of a detector block is dominated by the scintillation photon statistics and noise level of the photo detectors. Also, the input to the front-end processing is currently the analog anode currents of photomultiplier tubes (PMTs) because of the high gain-BW product and low cost per area compared to solid-state photo detectors. But, because of the known gain/timing variation of PMTs with variable magnetic field [1], any combined magnetic resonance positron emission tomography (MR-PET) modality would require a solid-state photo detector. PET detector block designs have been described and implemented in the literature using APD photo detectors at moderate values of gain [2].

1.2 Motivation

The motivation for this work comes from the idea of implementing Avalanche Photo Diodes instead of Photo Multiplier Tubes in the detector electronics assembly and implementing digital pole-zero filters and CFD circuits.

The detector module has been previously developed and tested using standard Nuclear Instrument Module (NIM) based front-end electronics. The entire gantry infrastructure currently exists for histogramming and controlling PMT-based detector modules. The idea was to utilize as much of the architecture as possible from an existing commercial PET scanner so that the core development of new APD algorithms

could begin without requiring the additional overhead of a completely new architecture.

1.3 Scope of Thesis

This thesis will involve the analysis, development and design of a proof-of-principle prototype PCB which will process APD analog signals and feed them into an FPGA for signal processing. This development board will be useful for integrating digital time stamps into it, which will result in decreased channel cost and smaller area for a higher level of integration. It will also be useful as a prototype board for testing out various other design changes that can be done to improve aspects like timing and performance.

1.4 Organization of Thesis

Chapter 2 presents an introduction to Positron Emission Tomography and also the working principles of photo multiplier tubes and avalanche photodiodes. The functionality, history and working of PET have been discussed. Next, a detailed description of APDs and PMTs is presented and also the differences between the two devices have been explained.

Chapter 3 describes different blocks of the APD prototype board and the basic working of each block has been described. Basic filter principles, A-D converters, amplifiers and PCB layout issues have been described in detail.

Chapter 4 presents the design specifications of the board. The input signals specifications, the external interfaces, the clocking specifications have been described. The filters have been analyzed and designed and the calculations and simulation results have been exhibited. The measured results have also been shown.

Chapter 5 presents the conclusion and future work related to this board. The accomplishments of this thesis and suggestions and leads to future work have been presented.

2 POSITRON EMISSION TOMOGRAPHY

2.1 Positron Emission Tomography

2.1.1 Introduction

PET stands for Positron Emission Tomography. PET is a major diagnostic imaging modality which helps the doctors view the patient's internal organs and their functionalities. It is a nuclear medicine imaging technique and it produces a 2-D or 3-D image of the patient's positron emitter tracer concentration which is proportional to volumetric metabolic activity and often correlates to physical abnormalities. PET can give the doctor his patient's whole body image in just one scan. A prime feature of PET is that quantitative measurement of physiological or biochemical information such as metabolism, blood flow and neural transmission within the body can be performed. PET has been chiefly used in research and study on brain functions and other organ mechanisms.

Nuclear medicine is a subspecialty within the field of radiology that uses very small amounts of radioactive material to diagnose or treat disease and other abnormalities within the body. Nuclear medicine imaging procedures are noninvasive and usually painless medical tests that help physicians diagnose medical conditions [3]. These imaging scans use radioactive materials called a radiopharmaceutical or radiotracer. The activity of the material produces certain radiations and the images are

reconstructed from these radiations with the help of signal processing electronics and computers.

A typical PET scanner is shown in the figure 1.

Figure 1 A PET scanner [35]

2.1.2 PET Functionality:

PET provides tomographic images of a living body in the active state and allows early diagnosis of lesions and tumors by injecting pharmaceuticals labeled with positron-emitting radioisotope into the body and measuring their concentrations. Typical positron-emitting radio-isotopes used in PET are ^{11}C, ^{13}N, ^{15}O and ^{18}F. Typically several millicuries of a positron emitting radioactive tracer (^{18}F for Whole Body scanning) is injected into the patient and allowed to uptake. This material is carefully selected so as to have a short life and is harmless to the human body. This is generally in the form of a glucose, which closely resembles a natural substance used by the body. Different tissues in the body take up different radio nuclides and hence the radioactive substance used during a PET scan depends on the organ under investigation. This radioactive substance spreads throughout the area which needs to be investigated. The ^{18}F PET tracer follows a decay scheme involves positrons being emitted, which can be detected by measuring the subsequent annihilations. Positron emitting radioisotopes have an excess of protons. This unstable state ends once the excess positron (β^+) is emitted. It travels a certain distance before it undergoes an annihilation with an electron (β^-) creating a pair of nearly collinear 511keV gamma rays in opposite directions. This spatial uncertainty in the annihilation localization sets the limit to the detection precision of the scanner (i.e. implicitly to the PET spatial resolution). A positron is the anti-matter of an electron. When matter collides with its corresponding anti-matter, both are annihilated. So, when a positron meets and electron, the collision produces two Gamma rays having the same energy but going in opposite directions.

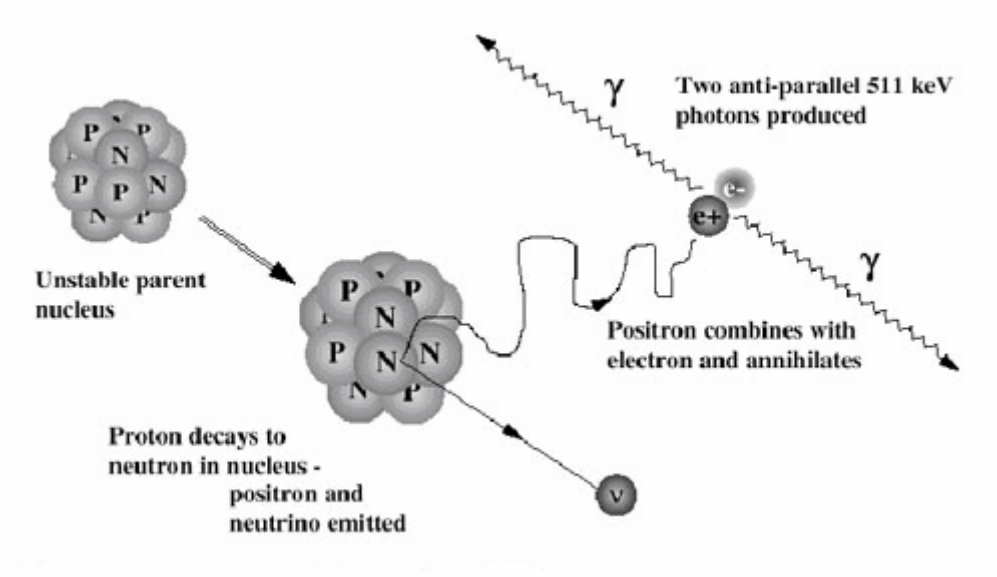

Figure 2 Anti-matter annihilation [34]

The number of positrons emitted by an organ or area of tissue indicates how much of the radioactive substance the organ or tissue has taken up and, therefore, how chemically active it is. Areas that take up more glucose are more metabolically active and appear brighter on a PET scan. Areas that don't use much energy or that are damaged don't take up as much glucose and therefore aren't as bright on a PET scan. Information from a PET scanner or gamma camera is processed and converted into images. A PET scan portrays chemical activity in parts of the body as images, or colors, of intensity. Areas of more intense color, or high uptake of the radioactive substance, are called hot spots. Areas of less intense color, which indicate a low uptake of the radioactive substance, are called cold spots.

2.1.3 History of PET

In the field of nuclear medicine, Positron Emission Tomography (PET) is relatively new. The concept of emission and transmission tomography was introduced by David Kuhl and Roy Edwards in the late 1950s. Their work later led to the design and construction of several tomographic instruments at the University of Pennsylvania.

PET was formally introduced to the medical community in the 1970s. In this period, Tatsuo Ido at the Brookhaven National Laboratory was the first to describe the synthesis of ^{18}F-FDG - the most commonly used PET scanning isotope carrier [4]. The compound was first administered to two normal human volunteers by Abass Alavi in August 1976 at the University of Pennsylvania. Brain images obtained with an ordinary (non-PET) nuclear scanner demonstrated the concentration of FDG in that organ. Later, the substance was used in dedicated positron tomographic scanners, to yield the modern procedure. The development of radiopharmaceuticals like FDG made it easier to study living beings, and set the groundwork for more in-depth research into using PET to diagnose and evaluate the effect of treatment on human disease.

In 1976, Dr. Michael Phelps established the first PET clinic for patient care at UCLA and from then on, the technology has gained a lot of popularity in the field of medicine [5] [6].

2.2 APDs and PMTs

The detection of low levels of light is the key process in medical imaging techniques based on radiation detection with scintillators. For nearly three decades, photomultiplier tubes have been used as photo detectors for single photon emission computed tomography (SPECT) and positron emission tomography (PET) applications and are still the most commonly used light detector in this field [7]. In recent years, compact semiconductor devices have become available that offer new design options and are competitive to PMTs in terms of performance and cost. Especially dedicated high-resolution applications, such as small animal positron emission tomography may benefit from these new detector technologies because compactness is a requirement.

The light that is isotropically emitted in the scintillation crystal needs to be collected efficiently by the photo detector. Hence, a good reflector and an optimized optical coupling between scintillation crystal and light detector are essential. Depending on the crystal size and shape, only a small fraction of the emitted light reaches the photo detector, which can be as low as 60% for a 10mm thick crystal (Moszynski et al., 1997). For common scintillators such as BGO, LSo or NaI (Tl), the light yield is in the range of only ~900photons/MeV to ~40000photons/MeV (NaI (Tl)) (Dorenbos et al., 1995). Because the light detector is at the beginning of the electronic chain low noise, high internal gain and required to achieve a high signal-to-noise ratio (SNR).

Light detectors are designed to convert low light levels into an electric signal of reasonable amplitude to avoid deterioration of the signal by external noise or pick-up. To ensure a high-quality signal, a light detector must have:

1. A high quantum efficiency—to transfer as many photons as possible into charge carriers to ensure high signal amplitude. (primary electrons produced to photons incident)
2. A fast read-out speed, for good timing resolution.
3. A good amplitude resolution that leads, in combination with a scintillator, to high energy resolution.

For low-light detection in the 200 – 1150nm range, the detector designer has three options, namely, Silicon PIN photodiode, Silicon avalanche photodiode and photomultiplier tubes [8].

Here we are implementing the Silicon avalanche photodiodes in the detector electronics of a Positron Emission Tomography scanner. The existing PET scanners utilize photomultiplier tubes in the detector electronics.

2.2.1 Photomultiplier Tubes

A photomultiplier tube is a vacuum tube consisting of an input window, a photo cathode, focusing electrodes, an electron amplifier and an anode usually sealed into an evacuated glass tube [7]. The structure of a PMT is shown below in figure 3.

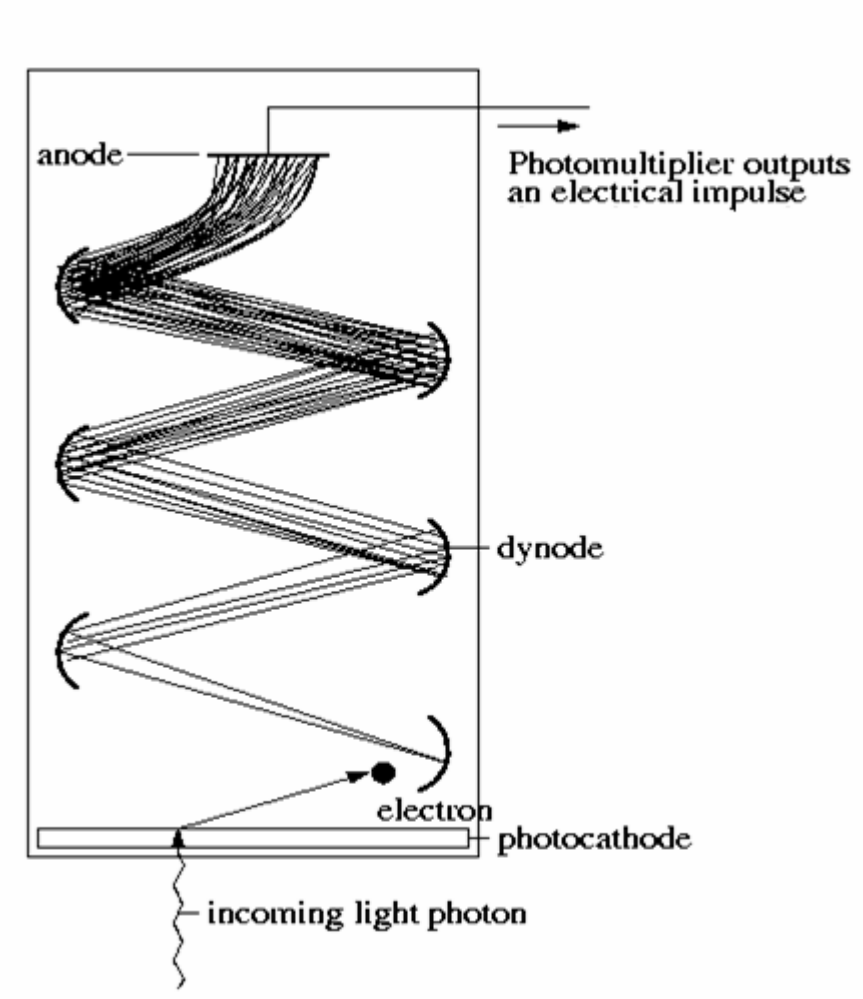

Figure 3 Structure of a Photomultiplier Tube[7]

Light which enters a photomultiplier tube is detected and produces an output signal through the following processes:

1. Light passes through the input window
2. Light excites the electrons in the photocathode so that photoelectrons are emitted into the vacuum. (external photoelectric effect)
3. Photoelectrons are accelerated and focused by the focusing electrodes onto the first dynode where they are multiplied by means of secondary emission. These secondary emissions are repeated at each of the successive dynodes.
4. The multiplied secondary electrons emitted from the last dynode are collected by the anode.

In emission tomography applications, PMTs are the most important light detectors. They are reliable and their high gain (upto 10^8) provides a very good signal-to-noise ratio.

They have drawbacks like low quantum efficiency (~25%) and sensitivity to even weak magnetic fields like earth's magnetic field. The most sensitive part of a PMT to magnetic fields is the electron collection structure in the front of the first dynode [7]. The photoelectrons are deflected from their trajectories and hence this results in decreased pulse height. The sensitivity to magnetic fields depends strongly on the type of the PMT, especially on the size of the entrance window, its shape and the dynode types. Small round PMTs are less sensitive than large rectangular tubes.

Meshed dynodes are less sensitive than other dynode types because of the short mean free path between two dynodes.

The PMT has remained the preferred detector for very low light applications because of its high internal gain.

2.2.2 Silicon Photodiodes

When light strikes special types of materials, a voltage may be generated, a change in electrical resistance may occur, or electrons may be ejected from the material surface. As long as the light is present, the condition continues. It ceases when the light is turned off. Any of the above conditions may be used to change the flow of current or the voltage in an external circuit, and hence may be used to monitor the presence of the light and to measure its intensity.

A photodiode is a semiconductor device which contains a p-n junction. Light absorbed in the depletion region or the intrinsic region generates electron-hole pairs, most of which contribute to a photo-current. The photo-current produced by a given level of incident light varies with wavelength. This relation between photoelectric sensitivity and wavelength is referred to as spectral response characteristic and expressed in terms of spectral sensitivity and quantum efficiency [8].

A typical Silicon photodiode cross-section is shown below in the figure 4.

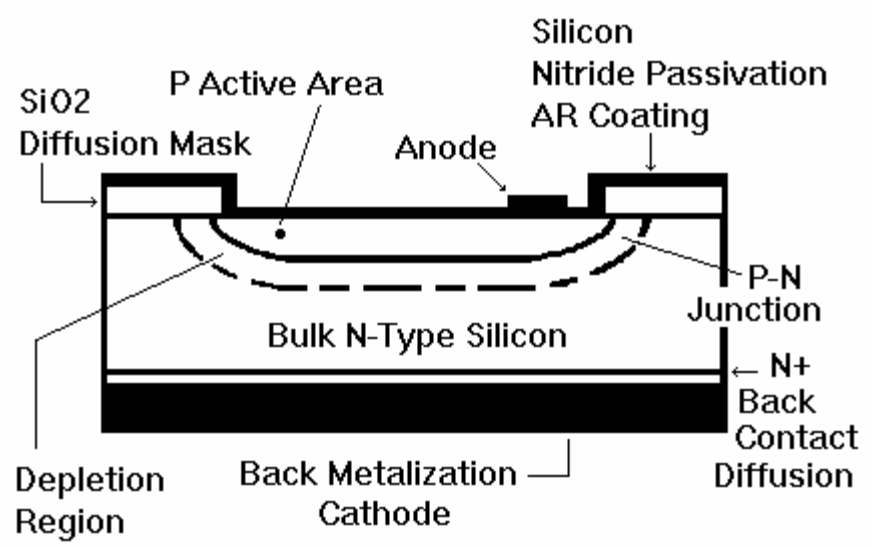

Figure 4 A typical Silicon photodiode cross-section [9]

The interface between the "p" layer and the "n" silicon is known as a pn junction. Small metal contacts are applied to the front surface of the device and the entire back is coated with a contact metal. The back contact is the cathode; the front contact is the anode. The active area is coated with silicon nitride, silicon monoxide or silicon dioxide for protection and to serve as an anti-reflection coating. The thickness of this coating is optimized for particular irradiation wavelengths [8].

The PIN photodiode is a compact, monolithic device, many times smaller and lighter than the PMT. It is the low-cost detector of choice for medium to high light level

applications [9]. However, the PMT has remained the preferred detector for very low light applications because of its high internal gain. Although PIN photodiode signals can be electronically amplified, their noise floor is typically three orders of magnitude higher than a PMT, limiting their ability to detect low light levels.

2.2.3 Avalanche photodiodes

APDs are semiconductor devices which show avalanche effect when subjected to a high reverse bias voltage. The internal current gain is a result of the avalanche effect. Avalanche photodiodes provide additional gain over PIN diodes by the generation of electron-hole pairs from an additional "avalanche" of electrons in the depletion region from the high electric field present.

Electronic Avalanche better known as avalanche breakdown, is the mechanism used to produce Zener or breakdown diodes, is a current multiplying process observed in strong electric fields, caused by the presence of high voltages within a semiconductor device.

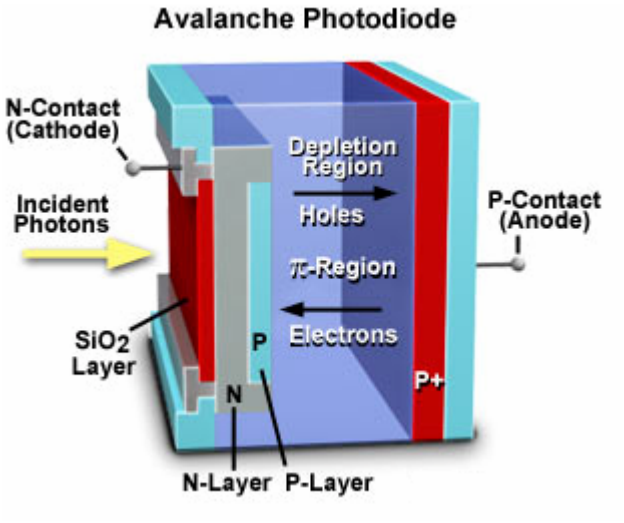

Figure 5 A cross-section of an Avalanche Photodiode [8]

The avalanche photodiode (APD) combines the benefits of both the detector types- PMTs and silicon PIN photodiodes; it is a silicon photodiode with internal gain [9]. Figure 5 schematically illustrates APD operation. As with a conventional photodiode, absorption of an incoming photon creates an electron-hole pair. A high reverse bias voltage (up to 2 kilovolts) creates a strong internal field; this accelerates the electrons through the silicon and produces secondary electrons by impact ionization. The resulting electron avalanche can produce gain factors up to several hundred. The important properties of APDs are:

1. High quantum efficiency
2. High internal Gain
3. Low dark current
4. Low bias voltage

Comparisons between PMTs and Semiconductor light detectors:

In comparison to PMTs, semiconductor light detectors used for scintillators readout provide the following advantages:

1. They are very compact, allowing the production of miniaturized detectors.
2. They are easy to produce as monolithic diode arrays for high-resolution applications.
3. They are insensitive to magnetic fields.
4. They are available with large active areas.
5. They have a quantum efficiency of upto 90% in the visible range.

The potential advantages of an APD detector over the conventional PMT based detectors are:

- Improved light collection efficiency(quantum energy).

  In a typical PMT, only 10-25% of incident photons are converted into photoelectrons at the photocathode, and even this efficiency is achieved over only a narrow spectral range. But in a LAAPD, the Q.E. can be as high as 90% throughout the visible and as high as 80% even at 1000 nm [9].
- Ease of crystal manufacture.
- The most obvious advantage of the LAAPD is that it is a rugged, compact, monolithic detector, whereas the PMT is a bulky, mechanically fragile glass tube. The LAAPD is therefore particularly advantageous in applications where

space is at a premium or where the detector may be subjected to shock or vibration.

- PMTs are extremely sensitive to stray magnetic fields that can perturb the path of the photoelectrons, whereas LAAPDs are insensitive to magnetic fields.
- PMTs also require long settling times after exposure to high light levels. Conversely, the LAAPD requires no settling time whatsoever.
- Another advantage of solid-state technology is higher dynamic range. In a PMT, increases in incident light level eventually cause a cloud of electrons to build up around the anode grid. This cloud exerts a repulsive force on the other electrons coming from the final dynode, thus limiting the linear response range of a typical PMT to about four orders of magnitude. On the other hand, the LAAPD provides a linear response range up to 10^6 [9].

PMTs do remain superior in one area however – internal gain. PMTs routinely deliver gains up to 10^6, whereas a cooled LAAPD can provide a gain of 350. PMTs can thus count single photons under optimum conditions, whereas LAAPDs have equivalent noise charge (ENC) corresponding to 25 electrons [9]. Indeed, the PMT is still the only detector for photon counting and ultra-low light level applications. However, these represent the minority (<10%) of traditional PMT applications. The majority of applications only need a gain of couple of hundred, including important OEM applications such as spectroscopy, laser ranging, radiation monitoring, material analysis, environmental monitoring and medical imaging systems such as PET

(Positron Emission Tomography) scanners. At these intermediate light levels, quantum efficiency is more important than gain in determining overall performance, which obviously favors the LAAPD [9].

2.2.4 APD Noise Specifications

When the signal is amplified, the inherent excess noise resulting from statistical current fluctuation in the avalanche multiplication process is generated [8].

The noise current is given by the following equation:

$$I = \sqrt{2qI_L M^2 FB} \qquad \ldots (2.1)$$

Where F=excess noise factor

M=Gain

I_L = Photocurrent at M=1

q = Charge of an Electron

B= Bandwidth

In photodiodes, the response speed is limited by the large load resistance. Hence it is not usually dominated by the thermal noise of the device. In the case of an APD, the gain can be increased until the shot noise reaches the same level as the thermal noise. Hence the APD can be used for an improved signal-to-noise ratio without affecting the response speed.

Figure 6 shows the noise specifications of an APD.

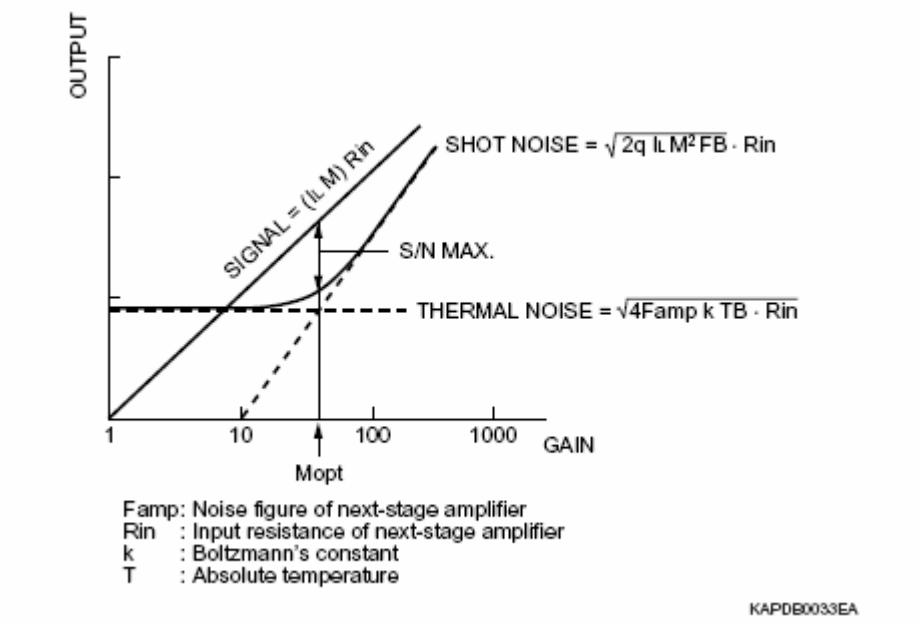

Figure 6 Noise specifications of an APD [8]

3 DESIGN BLOCKS

In this chapter, the building blocks of the APD prototype board will be discussed. The PCB layout issues will also be presented briefly.

3.1 Electronic Filters

3.1.1 Introduction to Filters

A filter is a device which rejects unwanted components in a system and can also be used to enhance useful components. Electronic filters are used to reject unwanted signal components and at the same time allowing the ones useful to for the application to pass through.

This circuit which has been designed to perform the needed frequency selection is called an electronic filter. Filters have many applications in the field of electronics. Frequency selection is a common process one has to adopt while designing most of the electrical circuits. Some of the most common applications are in signal processing circuitry and sound equalizers. Practically, all the applications of electronics need some sort of signal processing in their systems and hence filters are used extensively in electronics design.

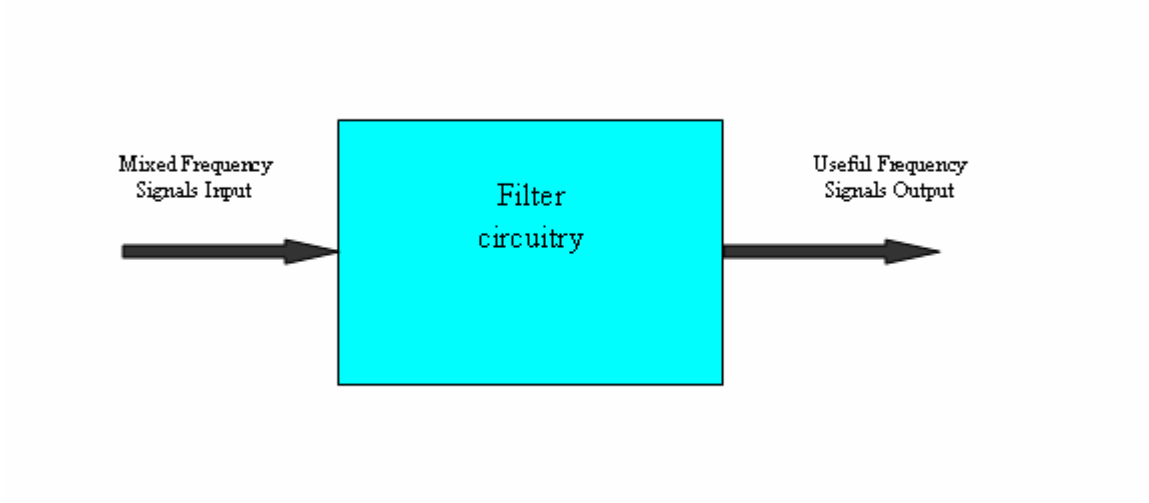

Figure 7 Block Diagram of an electronic filter

The basic filter block is shown in the figure 7 above.

3.1.2 Types of Electronic filters

Passive Filters:

Passive filters are the filters based on combinations of resistors (R), inductors (L) and capacitors (C). Proper use of these elements results in low-pass, high-pass, band-pass or band-stop filters. These types are collectively known as passive filters, because they do not depend upon an external power supply.

Active Filters:

Active filters are the filters which are implemented using both passive and active elements. The active element can be an operational amplifier. The specifications of the operational amplifier might have effects on the frequency of the filter. For example, the bandwidth of the operational amplifier might limit the upper frequency limit of the filter. Different combinations of elements results in different configurations of the whole system. These different configurations result in different functionalities.

Based on the functionality of the configurations, filters can be classified broadly into four categories:

1. Low-Pass filters
2. High-Pass filters
3. Band-Pass filters
4. Band-Stop filters

Low-Pass filters:

The low-pass filter, as the name suggests, makes an easy path for the low-frequency signals and at the same time makes a difficult path for the high frequency signals to pass.

Technically, a low-pass filter exhibits large attenuation for the high frequency signals and less attenuation for low frequency signals. A typical frequency response of a low-pass filter is shown below in figure 8:

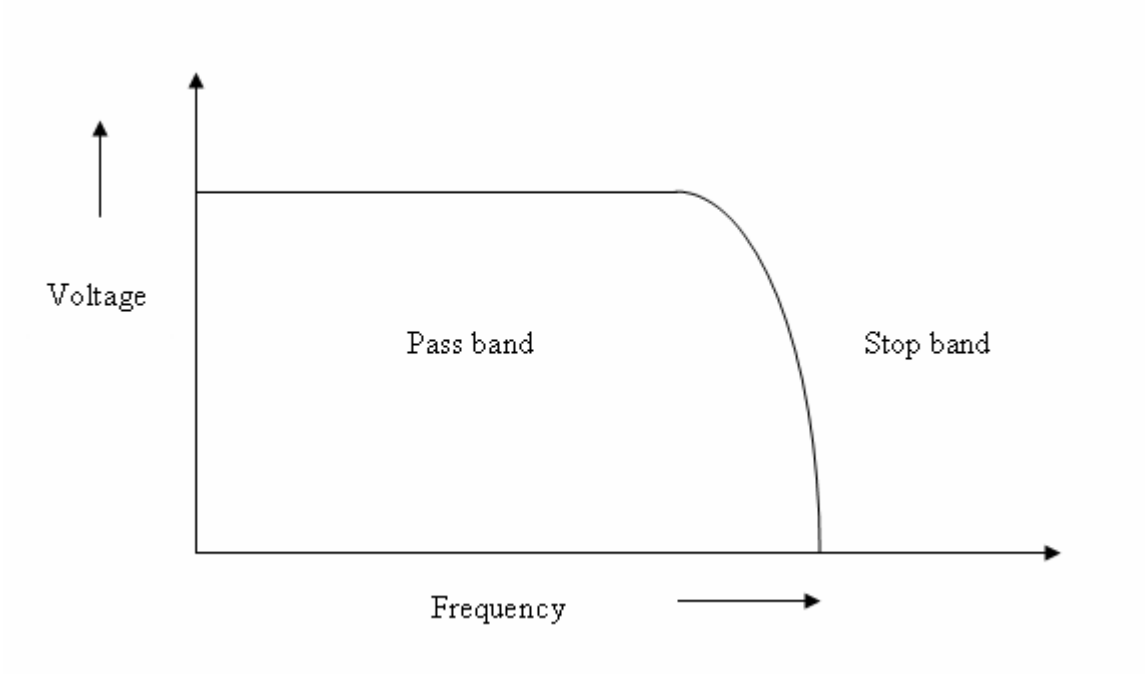

Figure 8 Frequency response of a low-pass filter

High-Pass filters:

High-pass filters function in quite the opposite way of that of the low-pass filters. These devices allow high frequencies to pass through easily and attenuate the low frequencies. A high-pass filter exhibits large attenuation for the low frequency signals and very less attenuation for high frequency signals.

A typical frequency response of a high-pass filter is shown below in figure 9.

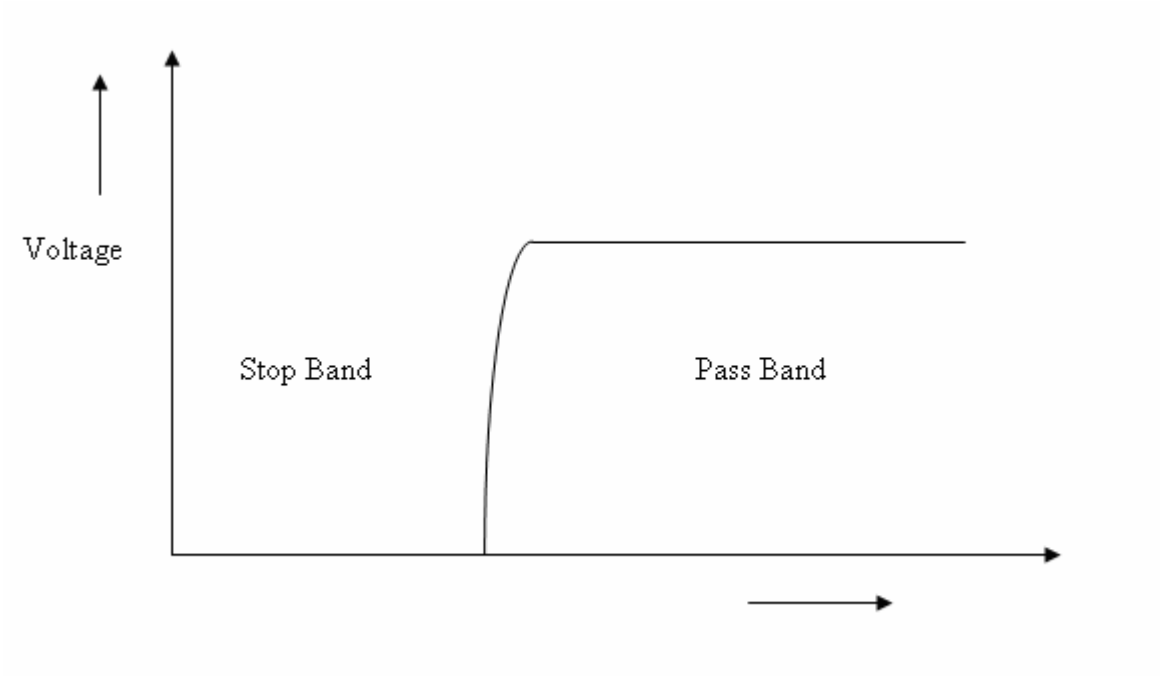

Figure 9 Frequency response of a low-pass filter

Band-Pass filters:

Band-pass filters are used to select a particular band of frequencies from a mixed frequency signal group. These filters are designed by combining the low-pass and high-pass configurations in series. In this way the frequencies below the lower limit and those above the upper limit of the band-pass filter will be attenuated, thus selecting a particular band.

Band-Stop filters:

Band-stop filters are useful for rejecting a set of frequencies from a wider range of mixed signals. They are a combination of low-pass and high-pass configurations in parallel. These filters will allow frequencies above the lower and upper limits of the design to pass through, thus “stopping” a band of frequencies.
Band-stop filters are also called band-reject filters or notch filters.

Typical frequency responses of band-pass and band-stop filters are shown as follows in figures 10 and 11.

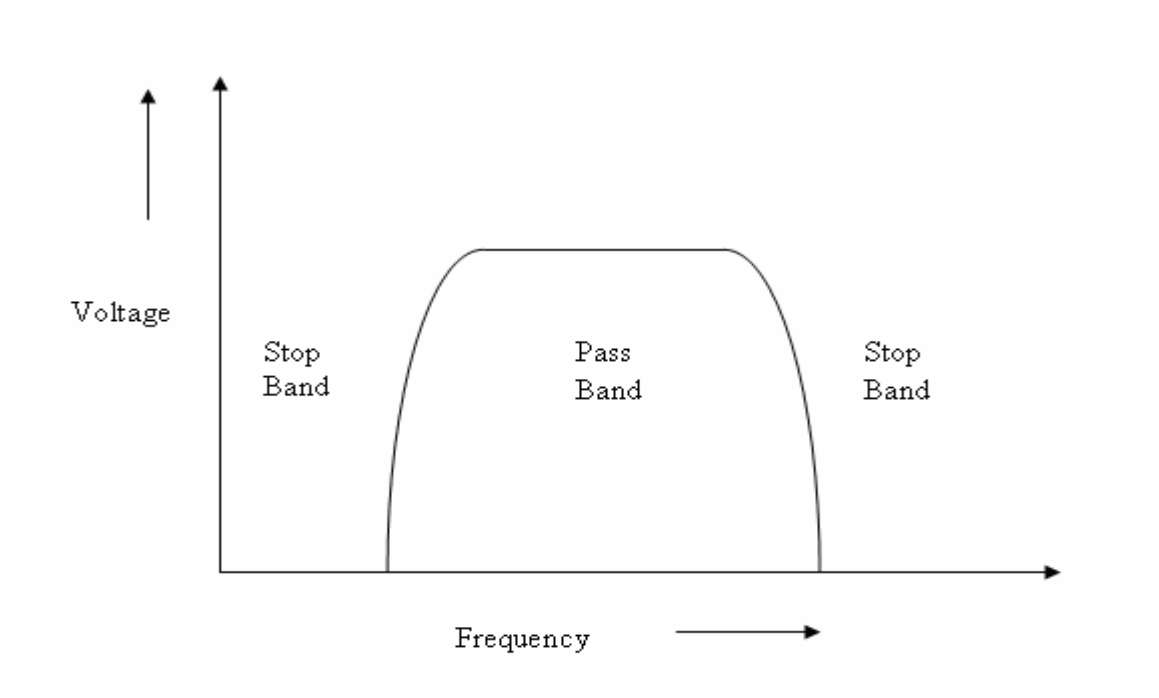

Figure 10 Frequency Response of a band-pass filter

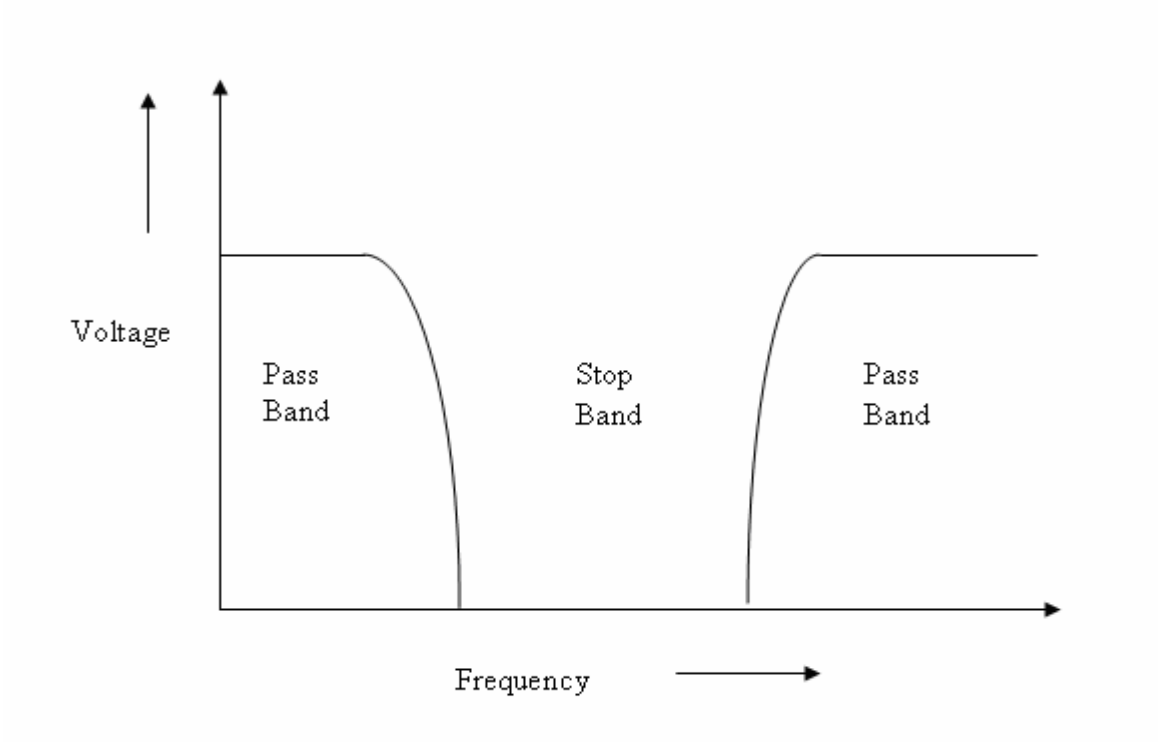

Figure 11 Frequency response of a stop-band filter

Single feedback filters:

The open-loop configuration of an amplifier not being practical, compensation networks come into play [10]. A compensation network is essentially a network which connects the output of the amplifier to one of the inputs. This output to input path can be used for several purposes: control output voltage, control gain, reduce distortion, improve stability, or even create instability, as in an oscillator. A single feedback loop is said to be employed when there is only one single path from the output to the input of the amplifier. The feedback networks can be passive, i.e., it consists of passive elements like resistors, capacitors, inductors etc. A typical single feedback configuration is shown below in figure 12.

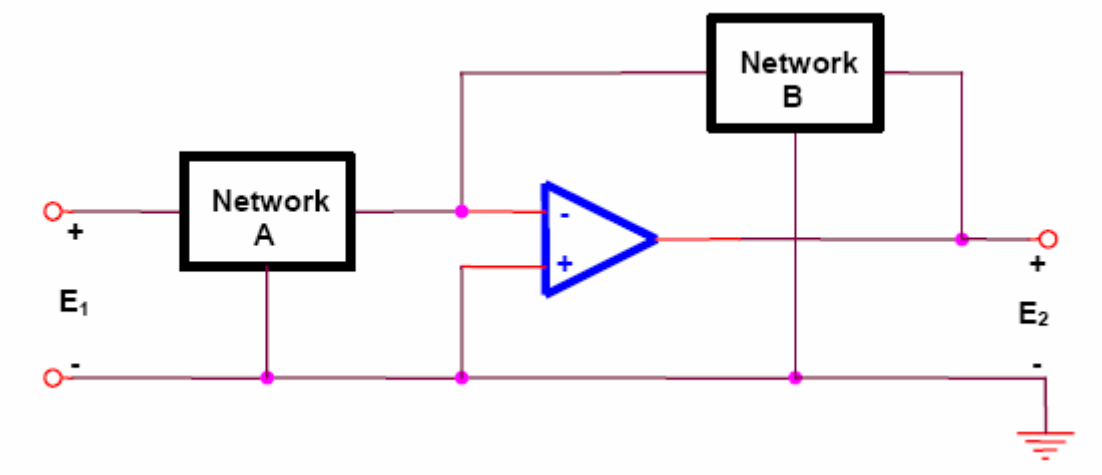

Figure 12 A typical single feedback active filter [10]

Network A is connected between the input of the circuit and input terminal of the operational amplifier. Network B is used as a feedback network from the output to the input of the operational amplifier.

The networks A and B being passive networks, different types of filter functionalities can be achieved. The use of resistors, capacitors and inductors, either some or all of them, can result in different bands of frequencies filtered out or allowed to pass through. The low-pass and high-pass configurations can be realized very easily and require least number of passive elements. The band-pass and the notch filter configurations, on the other side, require a relatively large number of passive elements for their realization.

The advantages [10] of a well-designed single feedback active filter would be:

1. The pole locations are completely determined by the passive elements. In other words, pole locations will remain relatively stable and independent of changes in the active element.
2. The circuit is capable of summing signals at the input.
3. The circuit may be used to drive other networks without the usage of an isolating stage and without significant changes in circuit characteristics due to loading.

The disadvantages of a single feedback filter would be:

1. This circuit requires a large number of passive elements.

2. Bridged-T and twin-T networks must be used to produce the complex conjugate poles. Adjustment / trimming would be difficult and is not desirable because passive elements interact highly in these networks.
3. Limited high-frequency range is comparison with conventional passive filters.
4. Stability of closed loop is not guaranteed.

3.1.3 Multiple Feedback filters

A multiple feedback filter is a filter configuration where the operational amplifier is still the active element but there are more than one feedback paths around it. The elements which impart the filter its characteristics are again two terminal passive elements which constitute the feedback paths. The operational amplifier is normally used in the inverting configuration, with its non-inverting input terminal grounded.

The multiple feedback configuration results in a single pair of complex conjugate poles and zeros located only at the origin of complex frequency plane, or at infinity [10]. A maximum of five elements is necessary in order to realize the low-pass, high-pass and band-pass configurations. The multiple feedback filter configuration uses the operational amplifier as an integrator. Hence, the dependence of transfer function on the operational amplifier parameters is greater than in the Sallen-Key realization. Also, the multiple-feedback filter will invert the phase of the signal [10]. This is equivalent to adding the resultant 180 degrees phase shift to the phase shift of the filter itself.

A typical multiple-feedback configuration is shown in figure 13.

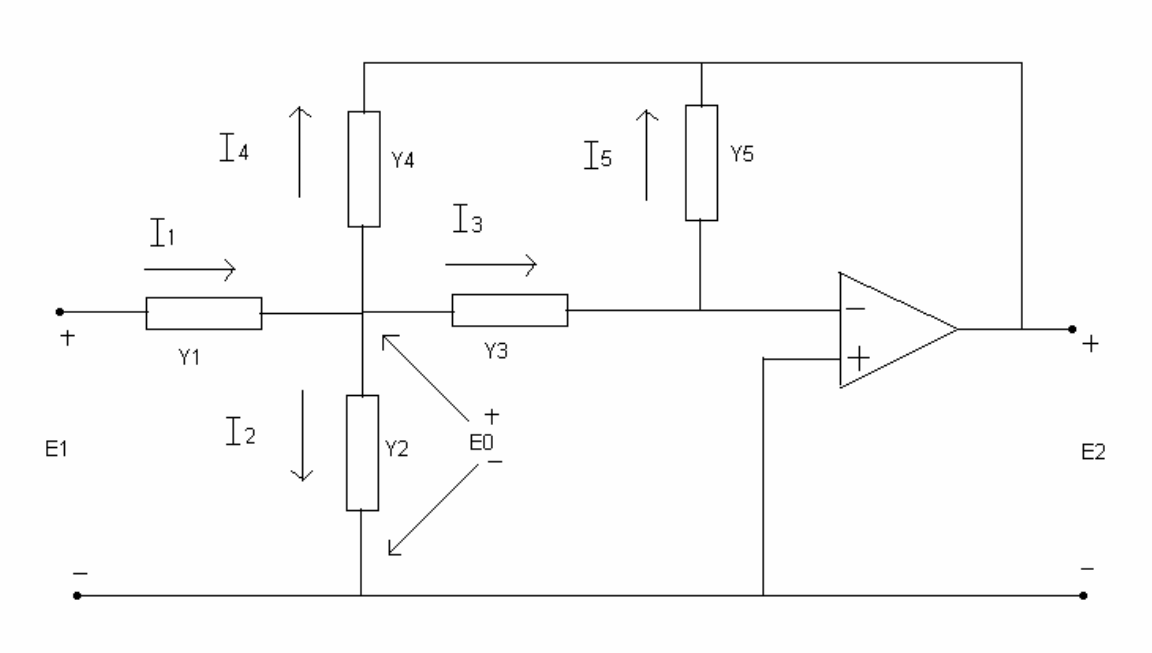

Figure 13 A typical Multiple feedback active filter

This basic circuit is used to realize voltage transfer functions with a single pair of complex conjugate poles and with zeros restricted to the origin or infinity.

The transfer function of the above circuit can be realized as follows:

Each of the elements Y_j represents an admittance of a single resistor or a capacitor. E_0 is the interior voltage as shown on the figure. I_j are the reference currents.

From Kirchhoff's Law, we can write

$$I_1 = I_2 + I_3 + I_4 \qquad \ldots (3.1)$$

Due to the virtual ground of the operational amplifier, the voltage across both Y_2 and Y_3 equals E_0. Hence, we can write,

$$I_2 = Y_2 E_0 \quad \ldots (3.2)$$

$$I_3 = Y_3 E_0 \quad \ldots (3.3)$$

$$I_4 = Y_4 (E_0 - E_2) \quad \ldots (3.4)$$

Also, due to the virtual ground, $I_3 = I_5$

Hence,

$$I_3 = Y_3 E_0 = -Y_5 E_2 = I_5 \quad \ldots (3.5)$$

Now, from the figure, we can write that

$$E_1 = \frac{1}{Y_1} I_1 + E_0 \quad \ldots (3.6)$$

Substituting the values of I_2, I_3, I_4 into the equation of I_1 and then using it in the above equation, we get

$$\frac{E_2}{E_1} = \frac{-Y_1 Y_3}{Y_5 (Y_1 + Y_2 + Y_3 + Y_4) + Y_3 Y_4} \quad \ldots (3.7)$$

This is the open-circuit voltage transfer function of the above shown figure.

Now, to obtain a low-pass filter, the normalized voltage transfer function must be of the form:

$$\frac{E_2}{E_1} = \frac{-H}{s^2 + \alpha s + 1} \quad \ldots (3.8)$$

Where H is the pass-band gain and is a positive real constant.

If we compare the equations 3.7 and 3.8, in order to have a numerator which is not a function of "s", Y_1 and Y_3 must be resistors. Y_4 must be a resistor in order to realize the constant term in the denominator. Also, to obtain the "s^2" term in the denominator, Y_5 and Y_2 must be capacitors.

Next, we replace the mathematical variables with Laplace transformed admittances representing passive components in the following way:

$Y_1=G_1$

$Y_2=sC_2$

$Y_3=G_3$

$Y_4=G_4$

$Y_5=sC_5$

Hence the voltage transfer function will be transformed into the following Laplace transfer equation:

$$\frac{E_2}{E_1}=\frac{-G_1G_3}{s^2C_2C_5+sC_5(G_1+G_3+G_4)+G_3G_4} \quad \ldots (3.9)$$

Replacing the G with R, we get,

$$\frac{E_2}{E_1}=\frac{\frac{-1}{R_1R_3}}{s^2C_2C_5+sC_5\left(\frac{1}{R_1}+\frac{1}{R_3}+\frac{1}{R_4}\right)+\frac{1}{R_3R_4}} \quad \ldots (3.10)$$

The above equation is the voltage transfer function of a multiple feedback low-pass filter.

By knowing the cut-off frequency and the gain, we can choose the required passive components and then calculate the values of others accordingly.

3.1.4 Low pass filter in Sallen-Key configuration

Most of the filters require a Quality Factor (Q) greater than 0.5. This can be achieved by using a positive feedback. If the positive feedback can be controlled and localized to below the cut-off frequency of the filter, any value of Q can be achieved. Then, the only factors limiting Q will be physical constraints of power supply and component tolerances.

The Sallen-Key configuration is also called a VCVS (Voltage Controlled Voltage Source). The source here is theoretically an ideal operational amplifier. Its gain can be set with simply with a pair of resistors. When passive RC networks are used with this VCVS, we can obtain various network functions.

The cut-off frequency of the network can be changed with the change in values of passive components - resistors and capacitors. The gain remains unchanged all the time. Hence it is also referred to as a Constant-K Sallen-Key configuration.

A capacitor is used as a positive feedback element in the low-pass configuration whereas a resistor is used in the high-pass circuitry.

The Sallen-Key configuration results in the least dependence of filter performance on the operational amplifier performance. This is because the operational amplifier is configured as an amplifier instead as an integrator. This minimizes the gain-bandwidth requirements.

The configuration with impedance blocks is shown in the figure 14 below.

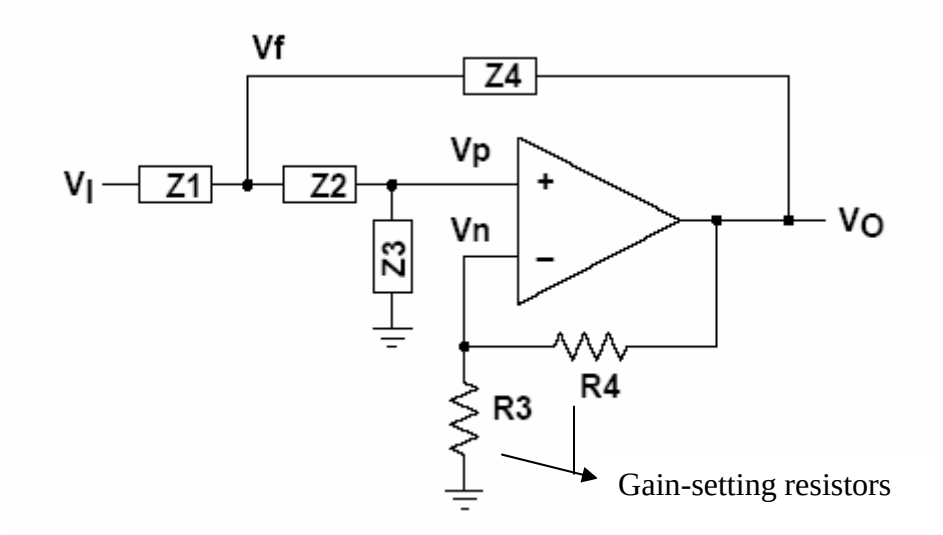

Figure 14 Op-amp in a Sallen-Key configuration

The derivation of the transfer function for this generalized circuit is shown below:

Applying KCL at the node Vf,

$$Vf\left(\frac{1}{Z_1}+\frac{1}{Z_2}+\frac{1}{Z_4}\right)=Vi\left(\frac{1}{Z_1}\right)+Vp\left(\frac{1}{Z_2}\right)+Vo\left(\frac{1}{Z_4}\right) \quad \ldots (3.11)$$

Applying KCL at Vp,

$$Vp\left(\frac{1}{Z_2}+\frac{1}{Z_3}\right)=Vf\left(\frac{1}{Z_2}\right) \quad \ldots (3.12)$$

From the above equations, we get

$$Vp=Vi\left(\frac{Z_2+Z_3+Z_4}{Z_2Z_3Z_4+Z_1Z_2Z_4+Z_1Z_2Z_3+Z_2Z_2Z_4+Z_2Z_2Z_1}\right)+$$

$$Vo\left(\frac{Z_1+Z_2+Z_3}{Z_2Z_3Z_4+Z_1Z_2Z_4+Z_1Z_2Z_3+Z_2Z_2Z_4+Z_2Z_2Z_1}\right) \quad \ldots (3.13)$$

Applying KCL at Vn,

$$Vn\left(\frac{1}{R_3}+\frac{1}{R_4}\right)=Vo\left(\frac{1}{R_4}\right) \quad \Rightarrow \quad Vn=Vo\left(\frac{R_3}{R_3+R_4}\right) \quad \ldots (3.14)$$

Solving the above equations, we get

$$\frac{Vo}{Vi}=\frac{K}{\frac{Z_1Z_2}{Z_3Z_4}+\frac{Z_1}{Z_3}+\frac{Z_2}{Z_3}+\frac{Z_1(1-K)}{Z_4}+1} \quad \ldots (3.15)$$

where $K = 1 + \frac{R_4}{R_3}$

The above equation is the ideal transfer function of the Sallen-key configuration with impedance terms.

Sallen-key Low Pass Circuit:

The above discussed circuit configuration can be configured as different network filters by replacing the impedance blocks by passive elements like resistors and capacitors accordingly.

For implementing a low-pass filter, the impedance blocks have to be substituted by the following:

$Z_1 = R_1$, $Z_2 = R_2$; $Z_3 = \frac{1}{sC_1}$; $Z_4 = \frac{1}{sC_2}$

The low-pass circuitry is shown in the figure 15.

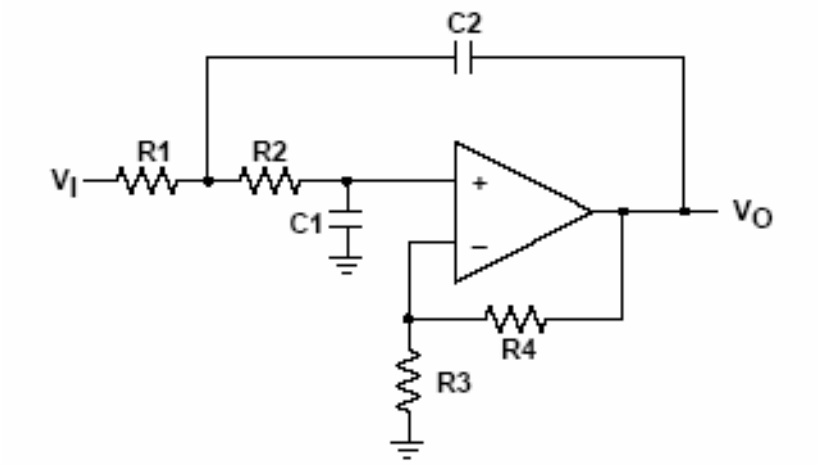

Figure 15 A low-pass filter in Sallen-Key configuration [10]

Substituting the values of the respective impedance in the transfer function equation, we get,

$$\frac{Vo}{Vp} = \frac{K}{s^2\left(R_1R_2C_1C_2\right) + s\left(R_1C_1 + R_2C_1 + R_1C_2\left(1-K\right)\right) + 1} \quad \ldots (3.16)$$

By letting $s = j2\pi f$, we get

$$f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \quad \ldots (3.17)$$

$$\text{and } Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_1 + R_1C_2(1-K)} \quad \ldots (3.18)$$

where f_c is the corner frequency and Q is the Quality factor.

By setting the resistors and capacitors accordingly, we can obtain the required corner frequency suited for a particular application.

3.2 A-D Conversion

3.2.1 Introduction

Most of the signals in the real world are analog. As needed by some applications, the analog signals are converted into digital signals so that they can be processed easily. The circuit which performs this operation is called an analog-to-digital converter.

An analog-to-digital converter is an electronic circuit which converts an input analog signal into a digital number. A digital number is in the form of bits (1's and 0's) and also in a particular format like 2's complement binary, Gray code, etc.

Digital signals are advantageous over their analog counterparts in many ways. The noise is a substantial factor in any analog signal. An analog signal can assume any value and hence cannot differentiate noise from the actual useful signal. In the digital case, there are only two options-either a 1 or a 0; anything else is discarded as unwanted. Hence noise reduction is an important feature of a digital signal. Another discriminating factor is the data compression. Digital data can be compressed into a very less space when compared to analog signals. The digital data can also be customized to perform many operations like self-correction, etc., which are not possible with analog signals.

Figure 16 Basic Block Diagram of Data Conversion

3.2.2 Sampling

As discussed above, the ADC converts an analog signal into digital signal, made up of binary bits. The most important and basic function of the ADC circuit is to sample the analog signal, so that each sample can be converted into a '0' or a '1' based on its voltage level.

The rate at which the analog signal is sampled is called the sampling rate. Shannon's sampling theory states than a continuously varying band limited signal can be sampled and that the original signal can be reproduced exactly from the discrete-time values. This recreated sampled representation's accuracy is limited by the ADC's quantization error and the band limiting Nyquist filters [11].

From basic logic, we can say that the more the number of samples of the signal, the more accurate is the reproduction of the signal. But more number of samples means more memory is required to store the samples. On the other hand, if the sampling rate is very low, the original signal cannot be accurately reproduced because the digital waveform will have only some points of the original signal. It is important to get a good number of samples of the analog signal because of the amplitude variations of the varying signal with respect to time [12].

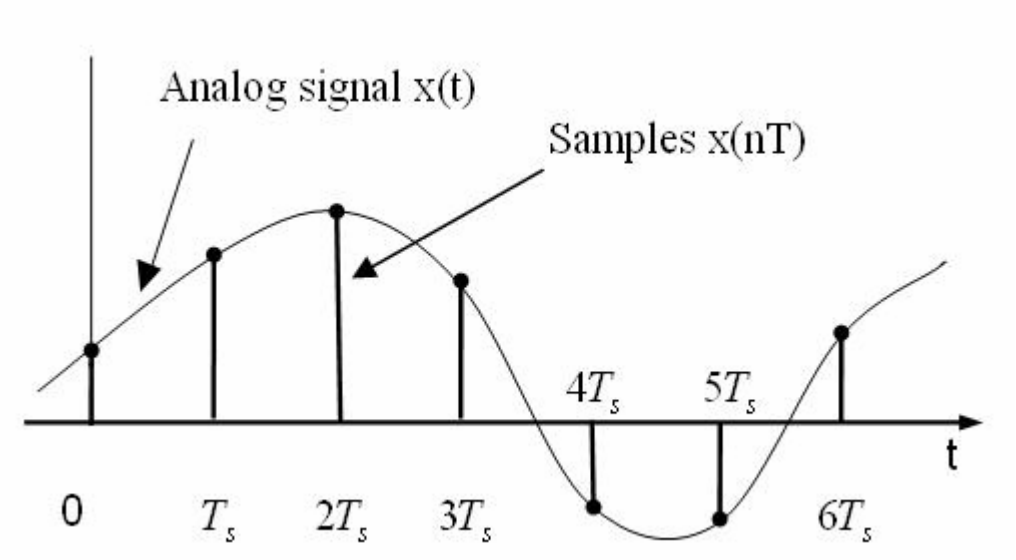

Figure 17 Sampling of an analog signal [6]

3.2.3 Sampling theorem

The sampling theorem gives us the knowledge about the best sampling rate to be used during analog-to-digital conversions to have the best storage/quality balance. It describes two processes in signal processing: a sampling process, in which a continuous-time signal is converted into a discrete-time signal, and a reconstruction process, in which the original continuous signal is recovered from the discrete-time signal.

A version of the theorem may be stated as “an analog signal that has been digitized can be perfectly reconstructed if the sampling rate was at least twice the highest frequency that is to be captured”.

The above mentioned statement is a very general way of looking at the sampling issue. Nyquist criterion [11] states that “The signal obtained from the reconstruction process can have no frequencies higher than one-half the sampling frequency. According to the theorem, the reconstructed signal will match the original signal provided that the original signal contains no frequencies at or above this limit.

In practice, the statements of the sampling theorem described above cannot be completely satisfied and also the reconstruction formula cannot be precisely implemented. The reconstruction process, in practice, involves summing terms to infinity and hence resulting in an interpolation error.

3.2.4 Aliasing

If the sampling theorem is not satisfied, the frequencies above half the sampling rate will be reconstructed as, and appear as, frequencies below half the sampling rate. The resulting distortion is called aliasing; the reconstructed signal is said to be an alias of the original signal, in the sense that it has the same set of sample values.

3.2.5 Resolution of an ADC

The resolution of the analog-to-digital converter indicates the number of discrete values it can produce over the range of analog values. The values are usually stored electronically in binary form, so the resolution is usually expressed in bits. In consequence, the number of discrete values available is usually a power of two. So, if you are using an 8-bit analog-to-digital converter, the lowest value will be zero and the highest value will be 255. If a 16-bit analog-to-digital converter is used, the lowest value would be zero and the highest value would be 65,535 [14]. Resolution can also

be defined electrically, and expressed in volts. The voltage resolution of an ADC is equal to its overall voltage measurement range divided by the number of discrete intervals. Again, the higher the number of bits, the higher is the amount of storage space needed and also higher is the quality achieved. One of the ways to know the necessary number of bits for an ADC is by calculating the desired noise level [14]. Since the values sampled from the original analog signal will several times need to be "rounded" to the nearest possible digital equivalent, this provides what is called quantization noise. The tolerable noise level depends on the application.

3.2.6 ADC Architectures

There are a whole lot of ADCs now in the market with different resolutions, bandwidths, architectures, packaging, power requirements, etc., customized for many different applications. All the applications have their own requirements and hence the variety in ADCs.

Architecture is the most basic parameter for any ADC. Some applications might work with an ADC of any architecture, but some would find only a particular architecture ADC to be useful. There are a lot of trade-offs made while deciding a particular

architecture for that particular application, and usually it is only the best choice for that application.

Some of the most used architectures today are:

- Successive approximations architecture
- Flash architecture
- Pipelined architecture
- Sigma-Delta architecture

Successive approximation architecture

A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved. At each step in this process, a binary value of the approximation is stored in a successive approximation register (SAR) [13]. The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons. An SAR converter conceptually uses a single comparator over many

cycles to make its conversion. It works like an old-fashioned balance scale [13]. Successive approximation is the architecture of choice for nearly all multiplexed data acquisition systems, as well as many instrumentation applications. The SAR ADC is relatively easy to use and has no pipeline delay. The architecture is shown in figure 18.

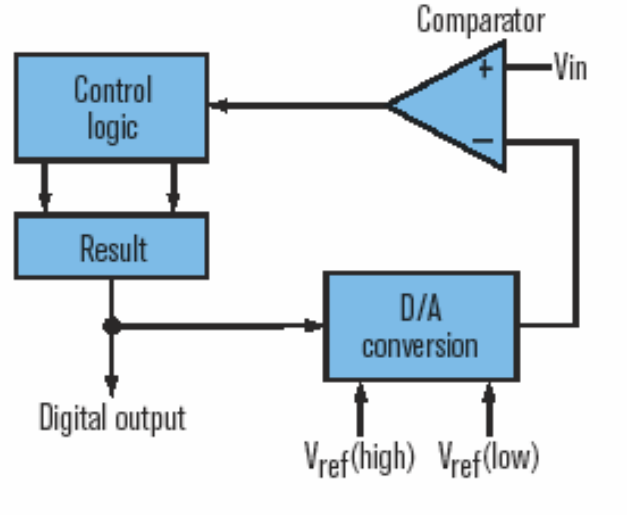

Figure 18 SAR ADC Architecture [14]

Flash Architecture

Flash architecture basically has a bank of comparators, each firing for their decoded voltage range [14]. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, but usually has only 8 bits of resolution (255 comparators - since the number of comparators required is 2^n - 1) or fewer, as it needs a large, expensive circuit. The flash architecture has the advantage of being very fast, because the conversion occurs in a single ADC cycle. The disadvantage of this approach is that it requires a large number of comparators that are carefully matched and properly biased to ensure that the results are linear. Since the number of comparators needed for an n-bit resolution ADC is equal to 2^n-1, limits of physical integration and input loading keep the maximum resolution fairly low [14].

They are suitable for applications requiring very large bandwidths. However, flash converters consume a lot of power, have relatively low resolution, and can be quite expensive. This limits them to high frequency applications that typically cannot be addressed any other way. The architecture is shown in figure 19.

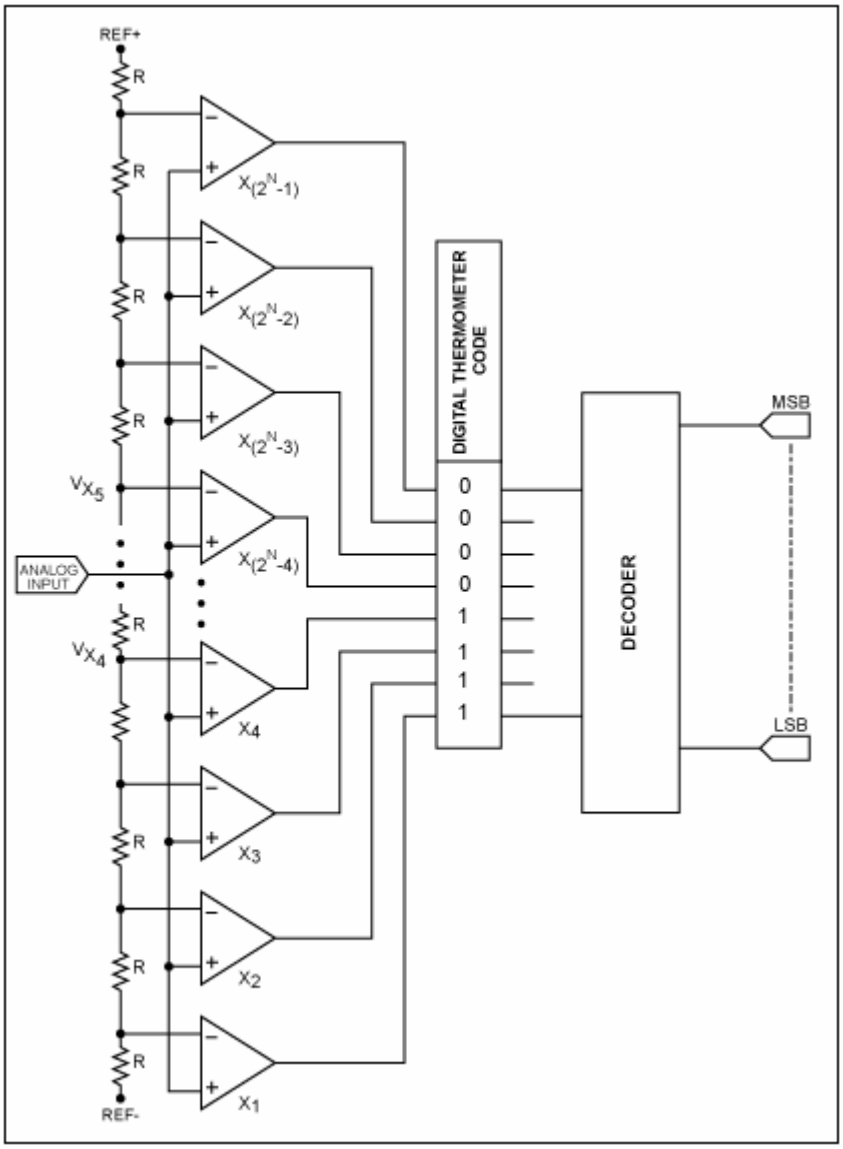

Figure 19 Flash ADC Architecture [14]

Pipelined architecture

A pipelined converter divides the conversion task into several consecutive stages. Each of these stages consists of a sample and hold circuit, an *m*-bit ADC (e.g. a flash converter), and an *m*-bit D/A converter (DAC). First the sample and hold circuit of the first stage acquires the signal. The *m*-bit flash converter then converts the sampled signal to digital data [14]. The conversion result forms the most significant bits of the digital output. This same digital output is fed into an *m*-bit digital-to-analog converter, and its output is subtracted from the original sampled signal. The residual analog signal is then amplified and sent on to the next stage in the pipeline to be sampled and converted as it was in the first stage. This process is repeated through as many stages as are necessary to achieve the desired resolution. By combining the merits of the successive approximation and flash ADCs this type is fast, has a high resolution, and only requires a small die size [14]. This class of ADCs is used in many types of instrumentation, including digital oscilloscopes, spectrum analyzers, and medical imaging. Other applications are video, radar, and communications applications and consumer electronics equipment, such as digital cameras, display electronics, DVDs, enhanced definition TVs, and high-definition TVs. The architecture is shown in figure 20.

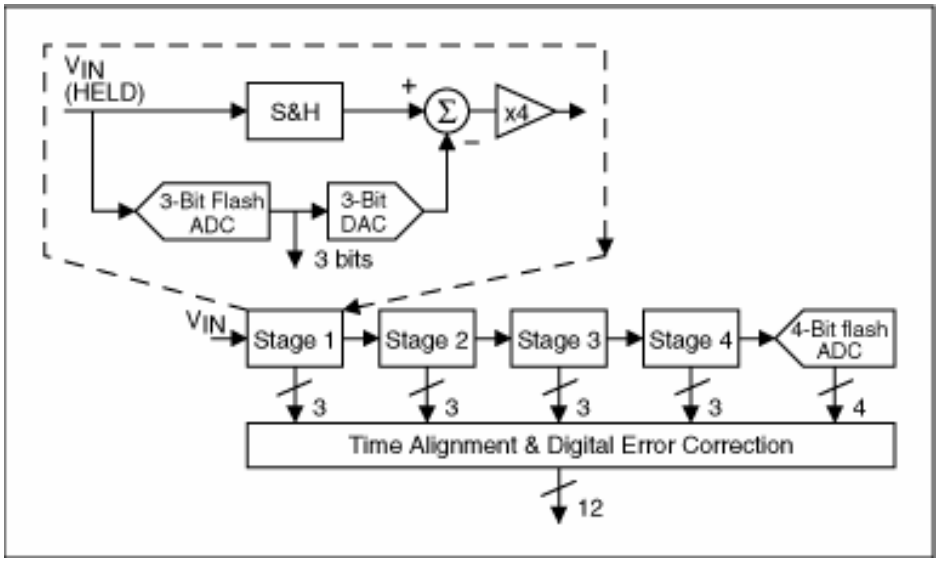

Figure 20 Pipelined ADC with four 3-bit stages(each stage resolves two bits) [14]

Sigma-Delta architecture

A sigma-delta converter consists of an integrator, a comparator, and a single-bit DAC. The output of the DAC is subtracted from the input signal. The resulting signal is then integrated, and the integrator output voltage is converted to a single-bit digital output (1 or 0) by the comparator. The resulting bit becomes the input to the DAC, and the DAC's output is subtracted from the ADC input signal, etc. This closed-loop process is carried out at a very high "oversampled" rate. The digital data coming from the ADC is a-stream of ones and zeros, and the value of the signal is proportional to the density of digital ones coming from the comparator. This bit stream data is then digitally filtered and decimated to result in a binary-format output [13]. One of the most advantageous features of the sigma-delta architecture is the capability of noise shaping, a phenomenon by which much of the low-frequency noise is effectively pushed up to higher frequencies and out of the band of interest. As a result, the sigma-delta architecture has been very popular for designing low-bandwidth high resolution ADCs for precision measurement [14]. The architecture is shown in figure 21.

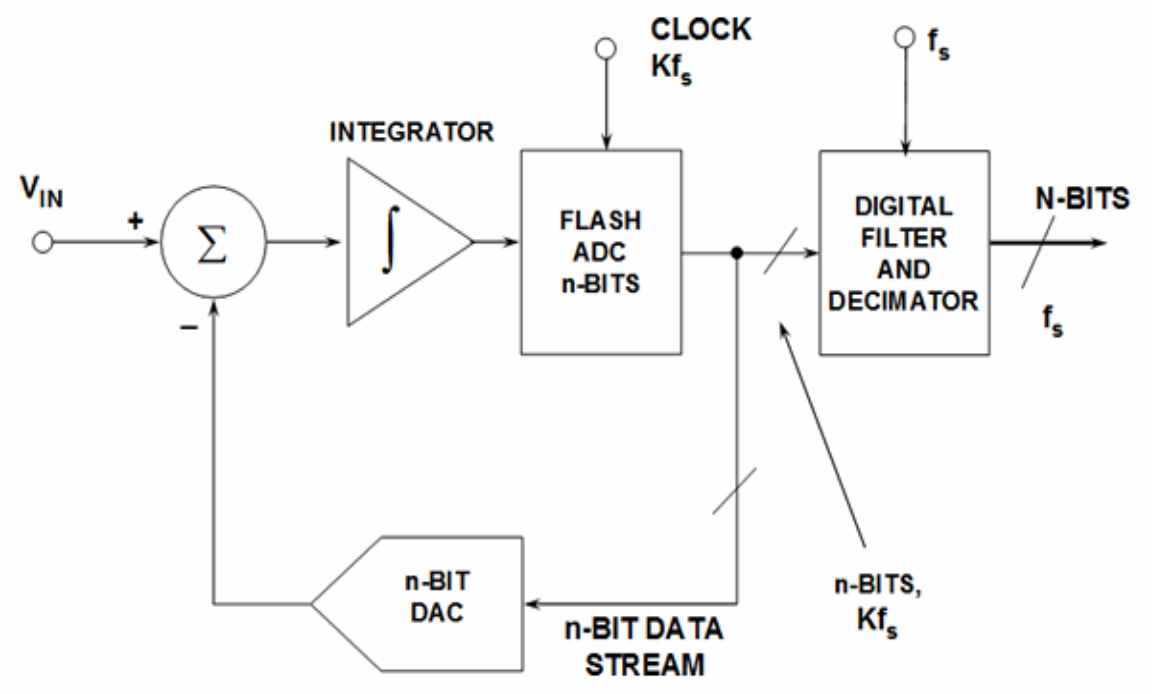

Figure 21 Multi-bit Sigma-Delta ADC [14]

3.2.7 Differential ADC driver

This section describes the methodology followed in selecting the best differential amplifier and then designing the driver circuitry to drive an analog-to-digital converter.

Driving an ADC is not a trivial job. The right high speed differential amplifier will add flexibility to signal chains that include a high speed Analog to Digital Converter (ADC). A differential amplifier can provide signal conditioning such as single ended to differential conversion, impedance transformation, and gain or attenuation [15].

ADCs are normally fixed gain devices that provide best performance when driven with signals that are just below, but not above, full scale. Digitizing small signals that have an amplitude measured in single digit multiples of the Least Significant Bit (LSB) reduces S/N ratio due to the quantization error becoming appreciable [15]. Similarly, driving an ADC beyond full scale causes obvious distortion. An op amp can be used to scale the signal to the best amplitude range for the ADC.

It is very important to first define the system requirements when it comes to choosing which amplifier to use for driving an ADC. Some important parameters are bandwidth, distortion, balance error, and settling time. BW and distortion will usually be the determining factors for wideband signals. For narrow band signals, bandwidth will drive the selection because distortion can be removed by the digital signal processing [15]. Narrow band signals are characterized by inter-modulation and harmonic distortion

products that fall out of band, while in a wideband signal many products will fall in band.

Nyquist criterion condition on the amplifier

The Nyquist theory sates that a signal must be digitized with an ADC that has a sampling rate of at least twice the highest frequency component of the sampled signal. The driving amplifier will be given very stringent criteria for Nyquist operation. The amplifier should have a 0.1 dB bandwidth of at least half of the sampling frequency [15]. The amplifier and ADC should also have comparable distortion and noise performance up to half of the sampling frequency. If the amplifier is to be used as an active filter, then the amplifier's −3 dB bandwidth should be close to two times the sampling frequency or more [4]. In general for Nyquist operation, the amplifier and the ADC should have comparable specifications for all parameters at frequencies of FS/2 and below.

Analog to digital converters often present challenging load conditions. They typically have high impedance inputs with large and often variable capacitive components [15]. As well, there can be current spikes associated with switched capacitor or sample and hold circuits. This makes an ADC input a challenge to drive. The output stage of a differential amplifier can help to smooth out current spikes as well as provide low impedance, fast settling source for accurate sampling.

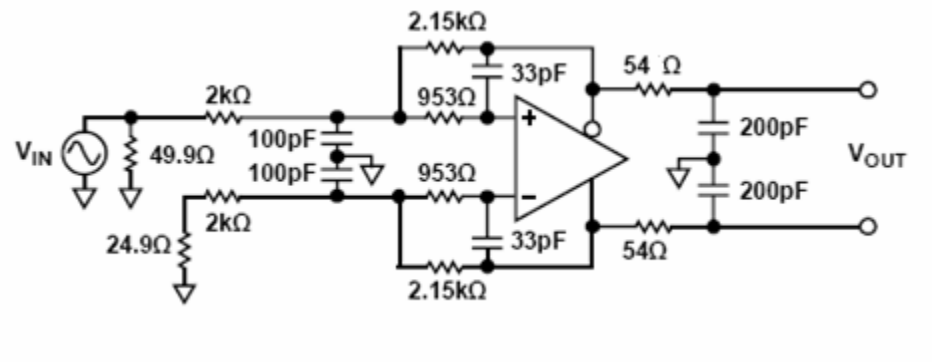

Figure 22 A typical Differential ADC Driver [15]

The above shown figure 22 is of a typical differential ADC driver, as well as a multiple feedback filter in this case.

The two 54 Ohm resistors serve to isolate the capacitive loading of the ADC from the amplifier to ensure stability. In addition, the resistors form part of a low pass filter, which helps to provide anti-alias and noise reduction functions. The two 200pF capacitors help to smooth the current spikes associated with the internal switching circuits of the ADC and also are a key component in the low pass filtering of the ADC input.

With all high-speed circuits, board layout is critical. The following points must be noted while considering the layout of the amplifier and ADC [15]:

- The amplifier and ADC should be located as close together as possible. Both the amplifier and the ADC require that the filter components be in close proximity. The amplifier needs to have minimal parasitic loading on the output

traces and the ADC is sensitive to high frequency noise that may couple in on its input lines.

- The ADC digital outputs should be well isolated from the ADC input as well as the amplifier inputs to avoid coupling between them.
- The amplifier and the ADC input pins should not be placed over power or ground planes to avoid parasitic capacitive coupling that may feedback undesirable signal to the input.
- Power supply bypass capacitors should be low ESR and placed within 2 mm of the associated pins.

3.3 FPGA

3.3.1 Introduction

FPGA stands for “Field Programmable Gate Array”. As the name suggests, it is a device, which has an array of programmable logic components called configurable logic blocks. These logic blocks are accompanied by programmable interconnect and they can be programmed to perform a variety of tasks on data fed in. Both, the interconnect and the configurable logic blocks, can be programmed by the designer for performing a large variety of functions and hence the part of the name “Field Programmable”.

Before programmable logic came into the picture, custom logic circuits were implemented at the board level using components and sometimes, at the more expensive gate level, as application-specific integrated circuits.

3.3.2 Basic Functionality of an FPGA

FPGAs contain a large number of logic blocks, as mentioned above, which can be viewed as standard components for building a logic circuit. The individual cells are interconnected by a matrix of wires and programmable switches. A user's design is implemented by specifying the simple logic function for each cell and selectively closing the switches in the interconnect matrix [16]. The arrays of logic cells and interconnect form a fabric of basic building blocks for logic circuits. Complex designs are created by combining these basic blocks to create the desired circuit.

The configurable logic clock architecture varies between different device families. Generally, each logic cell combines a few binary inputs to one or two outputs according to a Boolean logic function specified in the user program [16]. In most families, the user also has the option of registering the combinatorial output of the cell, so that clocked logic can be easily implemented. The cell's combinatorial logic may be physically implemented as a small look-up table memory (LUT) or as a set of multiplexers and gates. LUT devices tend to be a bit more flexible and provide more inputs per cell than multiplexer cells at the expense of propagation delay [16].

We will now explore the Spartan-3E FPGA of Xilinx Inc., which has been used in this particular prototype board. Sparatan-3E is the seventh family in the groundbreaking low-cost Spartan Series and the third Xilinx family manufactured with advanced 90nm process technology. Spartan-3E FPGAs deliver up to 1.6 million system gates, up to 376 I/Os and a versatile platform for FPGA architecture [16].

The architectural overview of the Spartan-3E FPGA is as follows:

The Spartan-3E family architecture consists of the following fundamental programmable elements:

1. Configurable Logic Blocks

   They contain flexible look-up tables (LUTs) that implement logic and also storage elements used as flip-flops or latches.

2. Input/output Blocks (IOBs)

   They control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow and the three-state operation. These blocks support a variety of state-of-the-art signal standards. Double data registers are also included in these blocks.

3. Digital Clock Manager blocks

   They provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

4. Multiplier Blocks

   They accept two 18-bit binary numbers and calculate their product.

5. Block RAM

   It provides data storage in the form of 18-Kbit dual-port blocks.

The Spartan-3E family architecture is shown in figure 23.

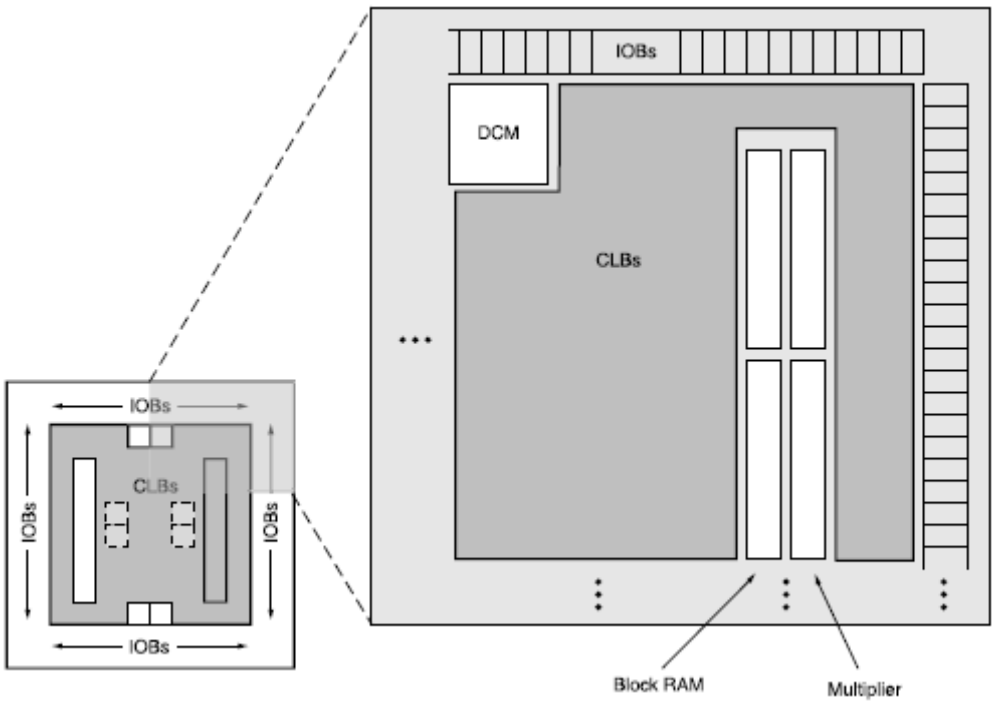

Figure 23 Xilinx Spartan-3E family architecture [16]

3.4 PCB Layout Issues

The quality of a signal on a printed circuit board is under scrutiny once the frequency of the signal transition increases. As the driver ICs switch faster and faster, more and more boards suffer from signal degradations like overshoot and undershoot, ringing, crosstalk and excessive settling delays. When these effects become serious enough, logic on a board can begin to fail.

When a low-frequency digital signal travels along aboard trace, the trace itself is “invisible” from a circuit standpoint [17]. But when a higher frequency signal travels along the same trace, the trace exhibits circuit characteristics that distort and degrade the signal. The problems get worse at high frequencies. For example, at gigabit speeds, signals are sometimes attenuated by a trace loss by more than 50% before arriving at the receivers [17].

The reason that fewer designs exhibited transmission-line effects more than a decade ago is that many of the ICs in use then switched more slowly than the ICs common today.

3.4.1 Flow of signals

In order to design high-speed boards, signal flows must be understood. Basically, when a current flows in a trace, there is an equal and opposite return current flowing in nearby copper. The return current flows whether we design a place for it to go or not, so it is best to always design that place by having a plane adjacent to the signal layer. The basic definition of a transmission line is a signal and its return path, and the return path defines a factor in the stack-up of the layers of a high-speed board [18].

Electromagnetic fields are always present when energy flows from one place to another, causing the return current (current must flow in a loop and return to its source). Fields are a major concern in high-speed designs because they change very quickly, which enhances their ability to interfere with everything else. Planes on adjacent layers minimize that effect [19].

3.4.2 Rise Time

A very important factor in high-speed designing is rise time. It is far more important than clock speed alone. By definition, rise time is the time needed for the signal to rise from 10% to 90% of its total amplitude as it turns on, or fall from 90% to 10% of its amplitude as it turns off. When the energy of a signal rises in a very short period of time, there are more harmonics at higher amplitude that must be dealt with. Plus, the frequencies of the entire bandwidth from the clock through the highest harmonics of the

signal must be considered. All this leads to the increased possibility of interference with everything around the signal. The knee frequency is the frequency above which harmonics present in the pulse edge can be ignored. The faster the rise-time, the higher the knee frequency and more important high quality terminators become [19].

The relation between knee frequency and rise-time is given by [19]:

$$KneeFrequency = \frac{0.5}{Risetime} \quad \ldots (3.19)$$

3.4.3 Crosstalk

Crosstalk occurs when two or more nets on a PCB are coupled to each other. Such coupling can arise any time two nets are routed next to each other for any significant length. When a signal is driven on one of the lines, the electric and magnetic fields it generates cause an unexpected signal to also appear on the nearby line due to either mutual inductance or capacitive coupling [17].

Crosstalk is the transfer of energy from an active source to a victim. Hence, the designer needs to know all the sources of noise inside the circuitry. As rise time shortens, the possibility of crosstalk increases dramatically [17]. Some other factors that increase crosstalk are close traces, wide traces, traces far from a return plane, traces crossing a split in a return plane and long traces without termination. Parts with a small signal swing are most susceptible to problems from crosstalk because they have less tolerance in their noise margin. Crosstalk must be avoided as much as

possible through intelligent and careful design. Extra spacing should be used around clock signals, memory circuits, periodic repeatable signals and switching power supplies. Internal routing of most nets is helpful. Limiting traces routed in a parallel manner either on a single layer or layer to layer will limit the buildup of crosstalk between them [17].

3.4.4 Reflections

Ideally, a signal traveling down a trace from a source to a load would have all the energy transferred to the load. It is not the case always. If there is too much energy to transition smoothly, a reflection forms in the opposite direction that can cause distortion to the original signal, false triggering to other ICs, and crosstalk and EMI problems to the area of the board [17].

Reflections are caused by inconsistent trace geometries, changes in routing like Y-splits, long stubs and fast signals on traces that are too long without termination. Reflection problems can be minimized by careful placement of parts to set up good routing schemes, limiting the length of high-speed traces to below termination length and using termination devices.

3.4.5 Termination

At high signal edge and/or transmission rates, Printed Circuit Board (PCB) traces behave like transmission lines with reflections occurring at all points along the trace where an impedance mismatch exists. These two impedance mismatches create

reflections which translate into more observable effects, such as signal ringing and stair-stepping. In turn, these distortions can cause false triggering in clock lines, cause erroneous bits on data, address or control lines, and contribute significantly to clock and signal jitter. Total emissions from the PCB are also increased resulting in EMI concerns [17]. Proper termination of these transmission lines can significantly reduce these effects and ensure proper system operation.

Termination devices absorb the excess energy at the load devices. Termination devices allow a signal's energy to be efficiently transmitted to a "distant" load across frequencies of interest. Several common termination techniques may be used; including Parallel, Thevenin, Series, AC and Schottky Diode. Each technique has both advantages and disadvantages.

The two major kinds of passive resistor termination are parallel termination and series termination.

Parallel termination devices control excess energy at the last load, and should be placed at or just beyond that load. They provide a constant logic level on the line, but are a constant DC load (power drain). Thevenin and RC terminations are forms of parallel termination.

Series termination [18], or backmatching, offers a simple, power saving solution with good signal integrity. It is a source end termination, versus a load end like the Parallel and Thevenin techniques. A series termination consists of a resistor connected

between the driver output and the line. The sum of the output impedance of the driver and the resistor value must equal the characteristic impedance. Because of the high impedance of the load, a reflection is still formed that causes the signal to double in strength, reaching the full voltage needed and thus to turn on the loads on the line. This is called reflection mode switching. The disadvantage in using series resistance is that it is difficult to select a crisp value for series resistance by application of the design equation.

3.4.6 Stack-up

The stack-up of a high-speed board can be critical and should be planned very early in the design process. Early planning will help set up layer paired routing - the routing of a signal trace on the layer adjacent to either side of a plane as it changes directions: N-S, or E-W [17]. This makes for a very clean return path, which contributes to good signal integrity. It is also important to have at least one good pair of power and ground planes very close together in the stack-up for high frequency capacitance.

3.4.7 Placement and routing

Placement and routing are also important issues. Parts should always be placed for best signal integrity as opposed to orientation conformity, and grouped by frequency, logic family, voltage and function. The routing strategy must be planned that will be used while the parts are being placed. The designer must know where the drivers and loads are to plan for the cleanest routing scenario. Signals should be routed within their own plane return areas so the return loop is small and the signals of one voltage do not

reference return planes of a different voltage. Signals should never be allowed to cross splits in reference planes [18].

3.4.8 Power Distribution structure

The power distribution structure of the board is also a factor of signal integrity, because if there is not sufficient power provided in the time frame needed, switching noise can result [17]. Capacitance in the form of caps and planes is needed to help supply power needs for the board. Bulk capacitors provide lots of low frequency power to the local capacitors and the planes and should be placed at the power input or the power supply. Local capacitors provide a source of higher frequency current, but in smaller amounts. They are generally placed very close to the power pins of the ICs. The highest frequency power is needed for the switching of the high-speed parts, and comes from the inter-plane capacitance, but in very small amounts [21]. Because of the inductance of the traces between the power pins and the planes, their connections should be as short and direct as possible.

4 DESIGN SPECIFICATIONS

In this chapter, the complete design specifications of the board have been presented along with simulation results followed by measured results.

4.1 Functionality and Block Diagram

The APD Algorithm Development board is basically a signal processing board and a part of the overall PET APD signal processing chain. The processing of the detector events is divided between two printed circuit boards: the analog subsection and control interface. The analog APD based prototype board connects to the detector interface through a twisted pair cable for receiving analog detector signals (T, L and E) and to the control interface for transmitting digital processed event data.

It is intended to implement APDs as detectors and also minimize additional crystal timing degradation caused by algorithm or analog processing. The main functions of the board are to process analog signals from the APDs at the input of the board to determine if a valid gamma ray event occurred, determine the crystal position and time of the event, and then transmit the event information to the control interface.

The block diagram of the prototype board is shown below in figure 24.

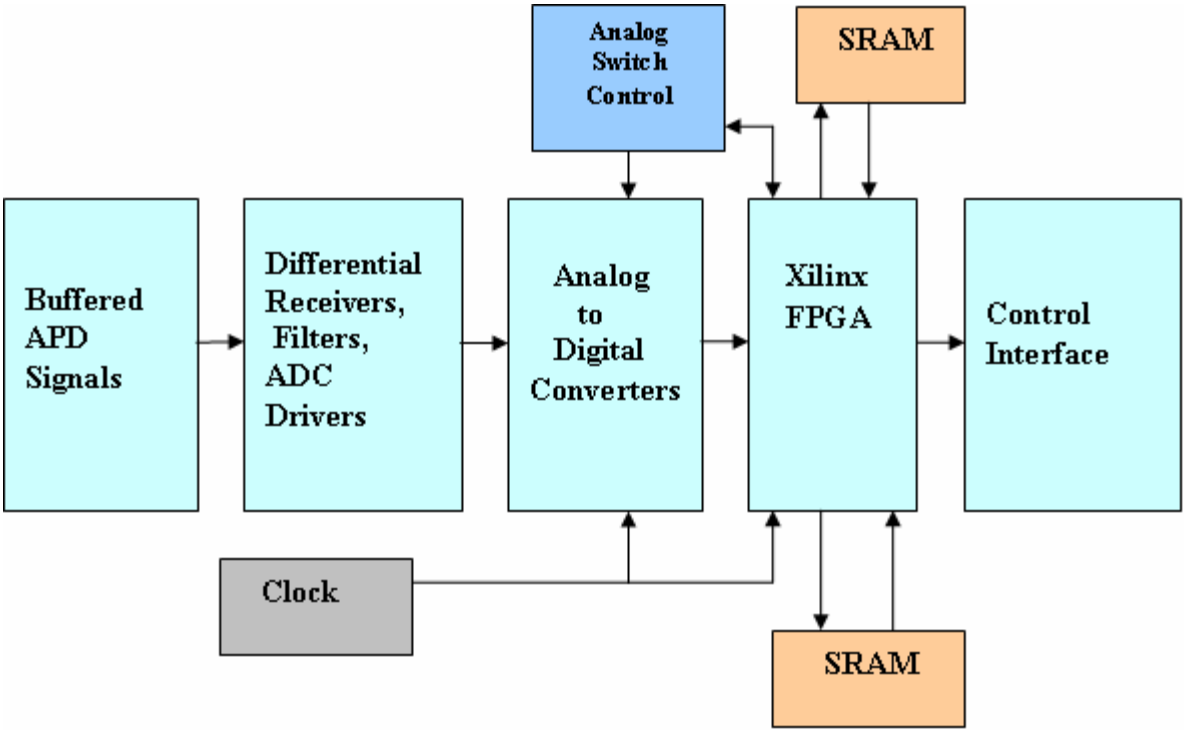

Figure 24 Block Diagram of the APD board

A brief description of the block diagram in reference to the board's functionality is given below.

The buffered APD signals in the form of voltages are received at the input of this board. These signals are properly filtered in order to be sampled into digital signals for further processing. The next stage is the ADC conversion, where the filtered APD signals are converted to digital words and then sent to the FPGA for further processing. The FPGA

interfaces with two SRAMs, processes data and send it out to the Control Interface board trough the connectors. The Control Interface in turn sends out data to the Co-incidence processor, which processes data at a higher level to determine coincident events.

4.2 External Interfaces

There are two external interfaces to this board. One is the detector cassette which inputs the buffered APD signals and the other is the Control Interface which takes in the output data of this board and sends it to a Coincidence processor. The two interfaces are described below:

1. Analog Subsection Interface:

   The APD prototype board acquires signals from the detector interface where the APD signals are filtered and buffered. They are brought up to a certain voltage level suitable for further filtering and eventually, ADC conversion.
   At the input of the board, each analog input connector will support two APD detector blocks of T, L and E signals using one shielded input connector. These APD detector blocks will be supported using twisted pair cabling.

   The board will have the capability to be DC or AC coupled from the detector module using a capacitor in each signal line. The cable termination at the analog

input to the APD algorithm board will be 100 Ohms resistive. Schottky diode protection will be provided at each active signal.

2. Control Interface

   The APD prototype board will be plugged into a Control Interface board, which will send data to the Coincidence processor. The Control Interface will have a positive voltage of 5V and 3.3V available for power.

4.3 Input Signals specifications

The inputs to the front-end processing are currently (not on this board) the anode currents of the photomultiplier tubes (PMTs).

Due to the gain/timing variation of the PMTs with variable magnetic field, any combined magnetic resonance positron emission tomography (MR-PET) modality would require a solid-state photo detector. PET detector block designs have been described and implemented in the literature using APDs as photo detectors at moderate gain values (~100). However, some Silicon APDs employ alternative doping and beveling techniques compared to traditional APDs that allow greater voltage to be applied(>1500V) before breakdown is reached and hence a greater operating gain(>1000) is achieved [8].

The APD algorithm prototype board receives buffered APD signals from the analog subsection interface through twisted pair cables.

Each of the APD block channels utilizes a differential signal of un-normalized T(X) and L(Y) used to derive the event crystal location based on Anger logic.

The peak amplitude is ideally 160mV for a full photoelectric interaction at 511KeV at the output of the charge sensitive preamplifier. This signal is low-pass filtered and amplified to a 250mV peak-peak differential level with common mode level of 0V. This is the defined input level to the APD development board analog input connectors.

The mean energy level received at the input of the prototype board will be 250mV (p-p), corresponding to a 511KeV photo peak at a scintillation crystal. The positive signal line from the differential driver will swing +125mV peak positive from the common mode level and the negative differential line will swing -125mV negative from the common mode level.

The common mode level from the detector cassette is analog ground. The signal energy level is set so that the accumulation of 4 pile-up events does not saturate the dynamic ranges of the T, L and E signals' ADCs. Both the T and L signal levels will assume a worst-case normalized position space value of 0-100% of the energy signal level.

The differential signal input to the APD algorithm prototype board will be minimally shaped from the charge sensitive preamplifier buffered output.

The T, L signals will be scaled for a 2V (p-p), 12 bit resolution ADC and E signals will be scaled for a 2V (p-p), 10-bit resolution ADC with the baseline set to mid-scale, neglecting the ADC inherent DC offset. Under this condition, ideally a 1V peak positive scale results in four photo peak events still within the ADC's dynamic range.

4.4 Signal Shaping and Amplification Specifications

4.4.1 The T and L Signals

The input T and L signals at the APD board will be first low-pass filtered using 40MHz filters. We use two filters each for T0 and T1. This is just a filtering stage and there is no signal amplification being done.

The component selected for the 40MHz filter is a surface mount device and has 8 pins. Pin1 is the signal input and pin8 is the filtered signal output. All other pins are tied to ground.

After this filtering stage, the signals are fed to a differential amplifier, which amplifies the signal to the required level. The amplified signal is then fed to a 5MHz Nyquist filter, which has been implemented in the multiple feedback low-pass filter configuration. This Nyquist filter also acts as an ADC driver.

4.4.2 The E signals

The E signals also are first fed to low-pass filters but the cut-off frequency is 80MHz in this case. The component chosen to perform this filtering is an 8-pole filter@80Mhz cutoff. After the low-pass filtering is done, the signals are then fed to a differential-to-single-ended converter to convert the differential E signals to single ended for further processing. These signals are then fed to a 2-pole Nyquist filter which is ideally programmable from 20MHz to 80MHz in steps of 20MHz.

The Nyquist filter has been implemented in the Sallen-Key low-pass filter configuration. There are two resistors at each frequency step which are to be varied so as to adjust the pole frequency accordingly. The use of potentiometers would induce huge capacitances resulting in the formation of poles and hence interfering with the performance of the filter.

Hence, in place of the two potentiometers, analog switch arrays are used. These switches have very low input capacitance (3.5pF) and on-resistance and also low off-capacitances. These switches are MOSFETs. The switches are implemented in the

circuit in a manner that a particular selection results in a particular resistance. The switch selection control is made available in the FPGA. Hence, the gate voltages can be defined from the FPGA and so a particular resistance can be chosen. So, in all, there must be four of these switch arrays, two each for the E0 and E1 signals.

After this Nyquist filter stage, these single ended signals have to be converted back to differential signals and also amplified in order to drive the ADC. For this purpose, they are now fed to a differential amplifier, which in this case, acts like a single ended-to-differential converter.

4.5 Filter Design

4.5.1 Multiple-feedback low-pass filter design

The 5MHz Nyquist low-pass filter for filtering T and L signals has been implemented in the multiple-feedback filter configuration. This filter also acts as an ADC driver. It drives the 80MSPS A-D converter.

The design of the 5MHz multiple-feedback filter is as follows:

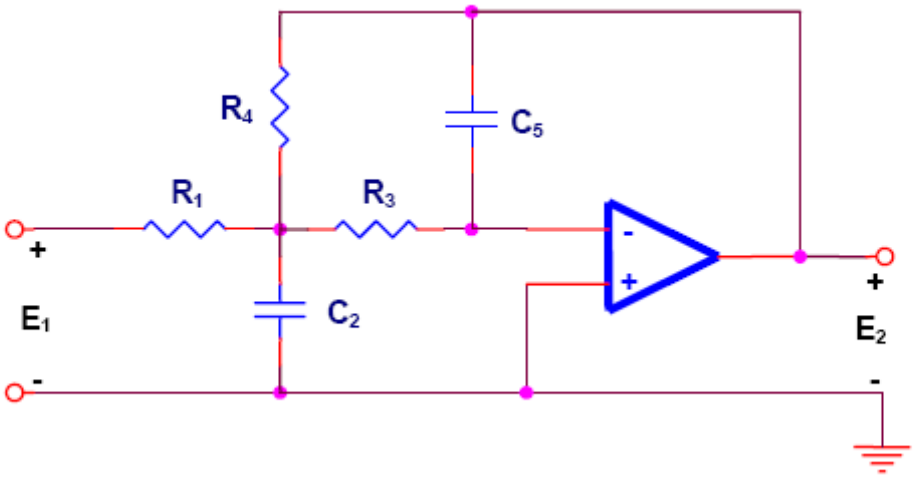

Figure 25 Multiple-feedback low-pass filter topology [10]

The transfer function will be in the form of:

$$\frac{E_2}{E_1} = \frac{-H\omega_0^2}{s^2 + \alpha\omega_0 s + \omega_0^2} \quad \ldots (4.1)$$

Where $A_0 = H$ and $\omega_0 = 2\pi f_0$

Comparing this equation with the transfer function derived before, we get the following equations:

$$C = \frac{k}{2\pi f_0} \quad \ldots (4.2)$$

$$H = A_0 \quad \ldots (4.3)$$

$\alpha = \sqrt{2}$ (for maximally flat response, 40dB/decade roll-off)

$$C_3 = C = \frac{k}{2\pi f_0} \quad \ldots (4.4)$$

$$C_2 = \frac{4}{\alpha^2}(H+1)\frac{k}{2\pi f_0} \quad \ldots (4.5)$$

$$R_1 = \frac{\alpha}{2Hk} \quad \ldots (4.6)$$

$$R_3 = \frac{\alpha}{2(H+1)k} \quad \ldots (4.7)$$

$$R_4 = \frac{\alpha}{2k} \quad \ldots (4.8)$$

Calculations are done as follows:

1. First, the value of C_5 is chosen to be 33pF.
2. The circuit has been designed for a gain of 2, and hence H=2.
3. The value of k is calculated.
4. Using the values of k, H and α, the values of C_2, R_1, R_3, and R4 are calculated with the help of the above mentioned equations.

The values obtained are rounded off to the nearest available market values, keeping in mind the performance.

The values obtained (and rounded off) are as follows:

C_5 = 33pF

C_2 = 200pF

R_1 = 348 Ω

R_3 = 225 Ω

R_4 = 698 Ω

The operational amplifier chosen is a differential driver.

4.5.2 Sallen-Key low-pass filter design

As mentioned in the above input signal specifications, the E signals are converted from differential to single ended signals to be fed to a programmable filter configuration. In this stage, the programmable filter is implemented in the Sallen-Key configuration. These low-pass filters have been programmed for 20, 40, 60 and 80MHz operations. They have been programmed by using analog switches whose control signals can be issued from the FPGA.

A Sallen-Key filter configuration is shown below in figure 26:

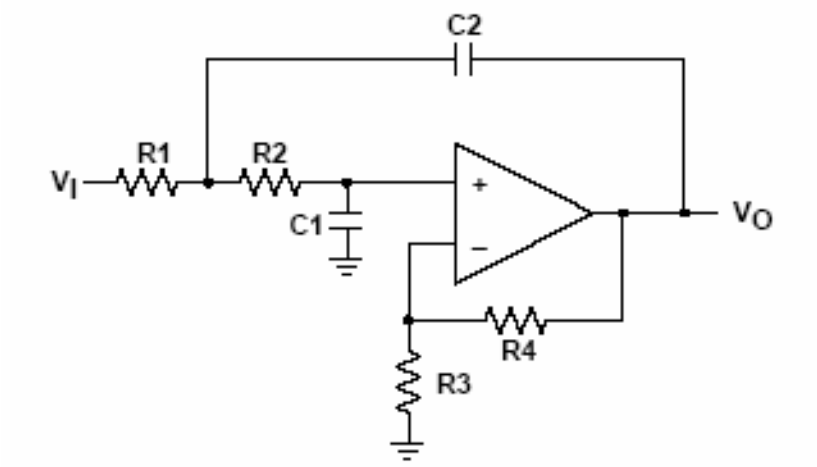

Figure 26 Sallen-Key low-pass filter topology [10]

The transfer function of a Sallen-Key filter configuration has been derived to be:

$$\frac{Vo}{Vi} = \frac{K}{s^2(R1R2C1C2) + s(R1C1 + R2C1 + R1C2(1-K)) + 1} \quad \ldots (4.9)$$

By letting $s = j2\pi f$, we get

$$fc = \frac{1}{2\pi\sqrt{R1R2C1C2}} \quad \ldots (4.10)$$

$$\text{and } Q = \frac{\sqrt{R1R2C1C2}}{R1C1 + R2C1 + R1C2(1-K)} \quad \ldots (4.11)$$

Now, we can simplify the above equations in more than one ways. One of the simplifications can be done by letting

$R_1 = mR$

$R_2 = R$

$C_1 = C_2 = C$

These substitutions result in the cut-off frequency equation to be modified to:

$$f_c = \frac{1}{2\pi RC\sqrt{m}} \quad \ldots (4.12)$$

And also,

$$Q = \frac{\sqrt{m}}{1 + 2m - mK} \quad \ldots (4.13)$$

Now, choosing m=2, and C=27pF, we can calculate the value of R for each of the frequencies of 20, 40, 60 and 80MHz.

From the value of R, we get the values of R_1 and R_2.

The Sallen-Key low-pass filter has been implemented in unity gain configuration. Hece the value of K will be 2.

The values of resistors for each of the four frequencies are as follows:

20MHz:

$C_1 = C_2 = 27pF$

$R_1 = 416\ \Omega$

R_2 = 208 Ω

40MHz:

$C_1 = C_2$ = 27pF

R_1 = 208 Ω

R_2 = 104 Ω

60MHz:

$C_1 = C_2$ = 27pF

R_1 = 138 Ω

R_2 = 69 Ω

80MHz:

$C_1 = C_2$ = 27pF

R_1 = 104 Ω

R_2 = 52 Ω

All the resistor values have been adjusted on the schematic by taking into consideration the on-resistance of the analog switches. The analog switches have an on-resistance of about 50 Ω.

The signals from these Sallen-Key programmable filters are fed in the ADC driver, where the signals are first converted from single-ended to differential and then amplified to the required voltage level in order to drive the A-D converter.

4.5.3 Simulation results of filter circuits

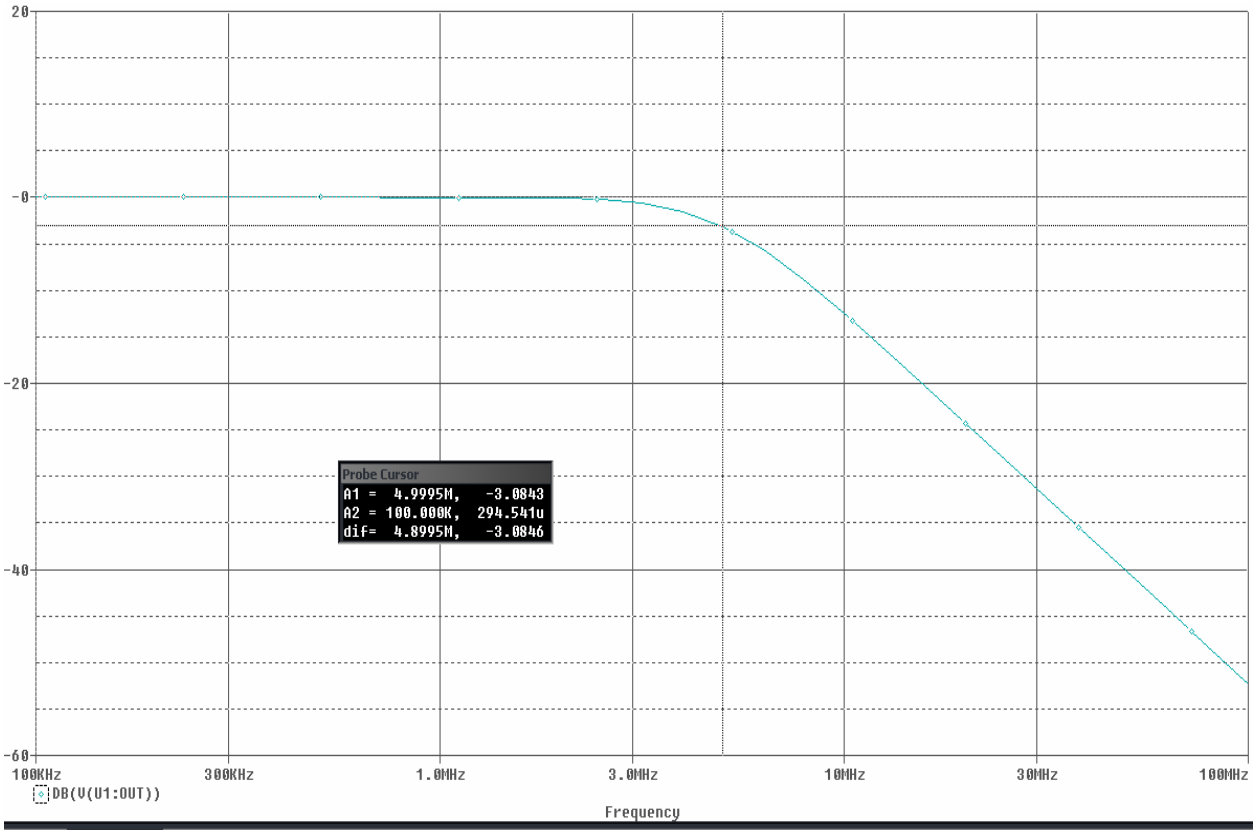

Figure 27 MFB filter response- Vout(dB) vs Frequency

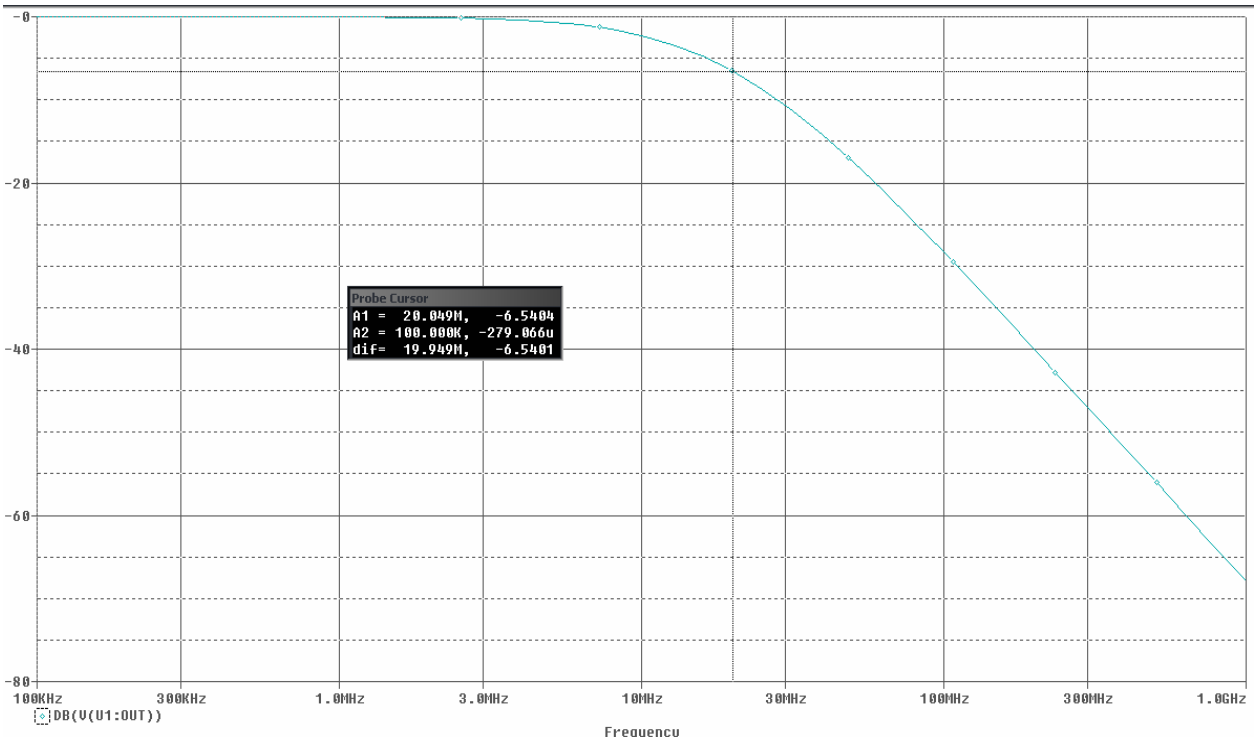

Figure 28 Sallen-Key LPF Vout(dB) vs Frequency—20MHz

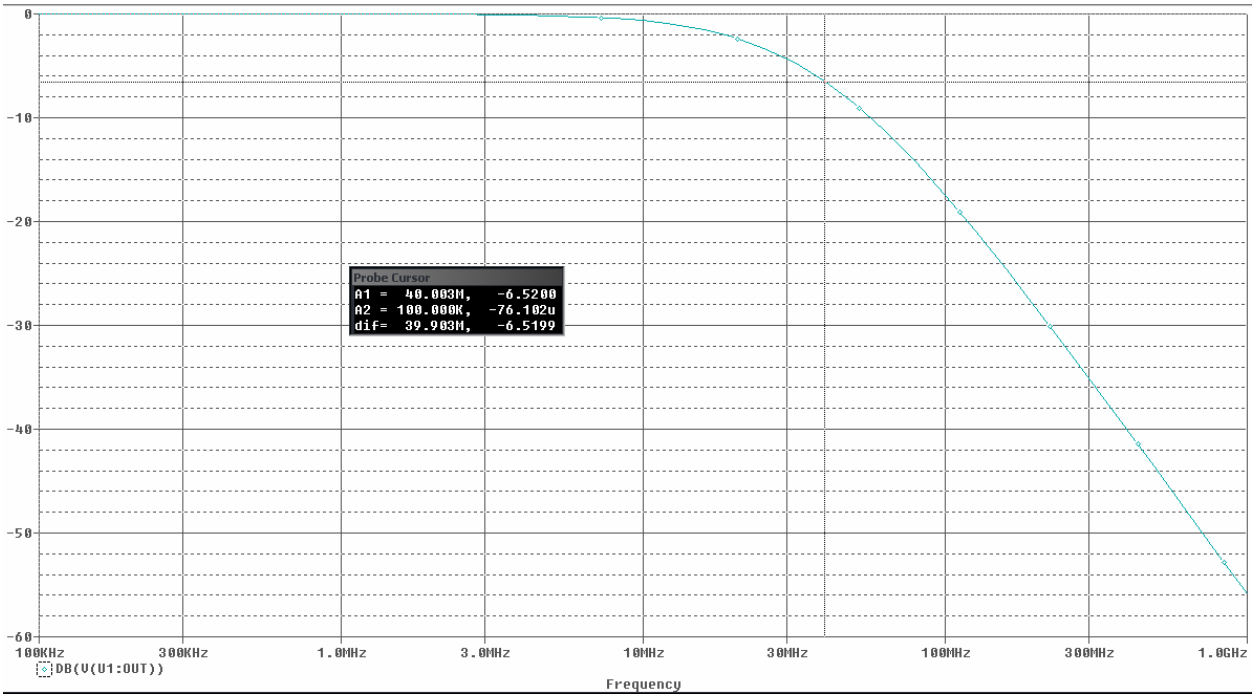

Figure 29 Sallen-Key LPF Vout(dB) vs Frequency—40MHz

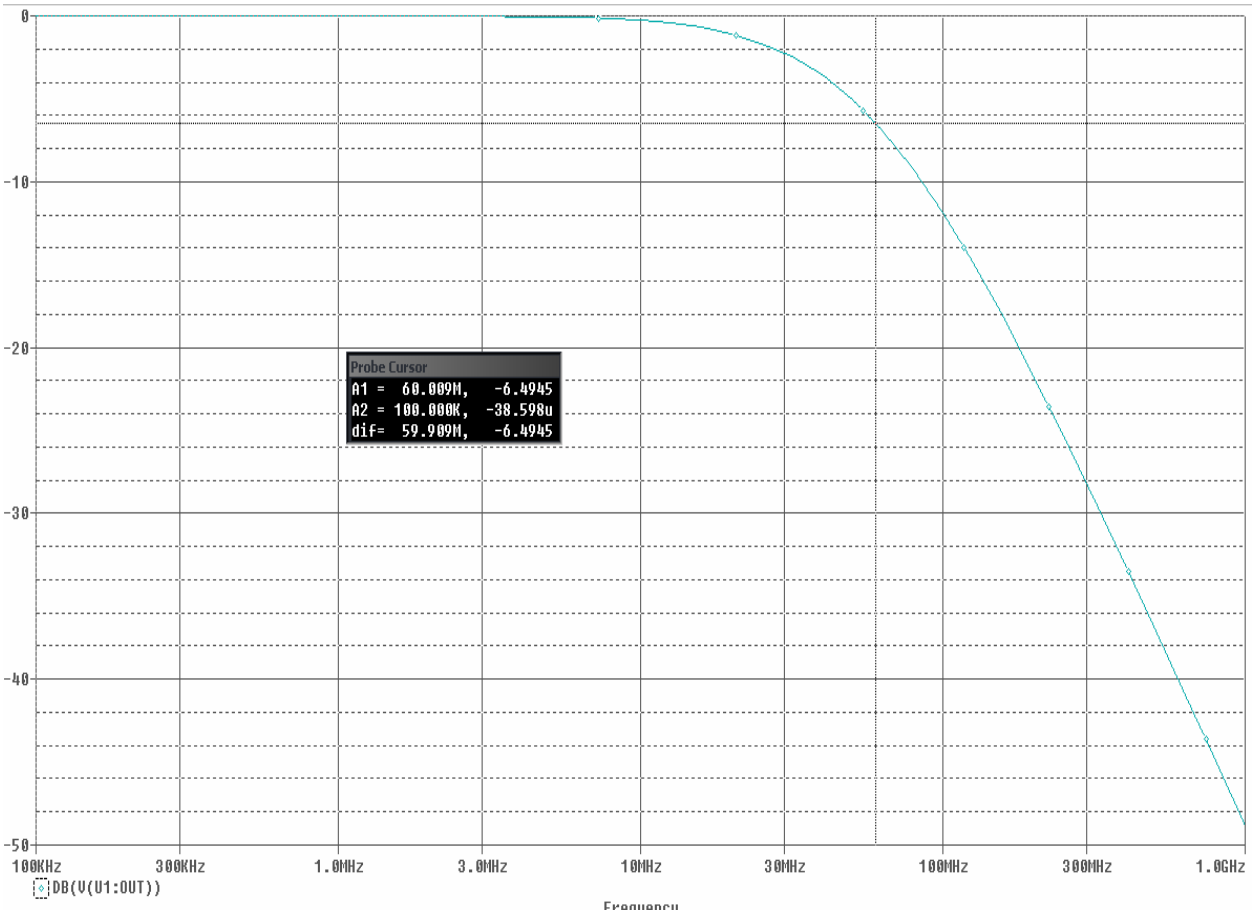

Figure 30 Sallen-Key LPF Vout(dB) vs Frequency—60MHz

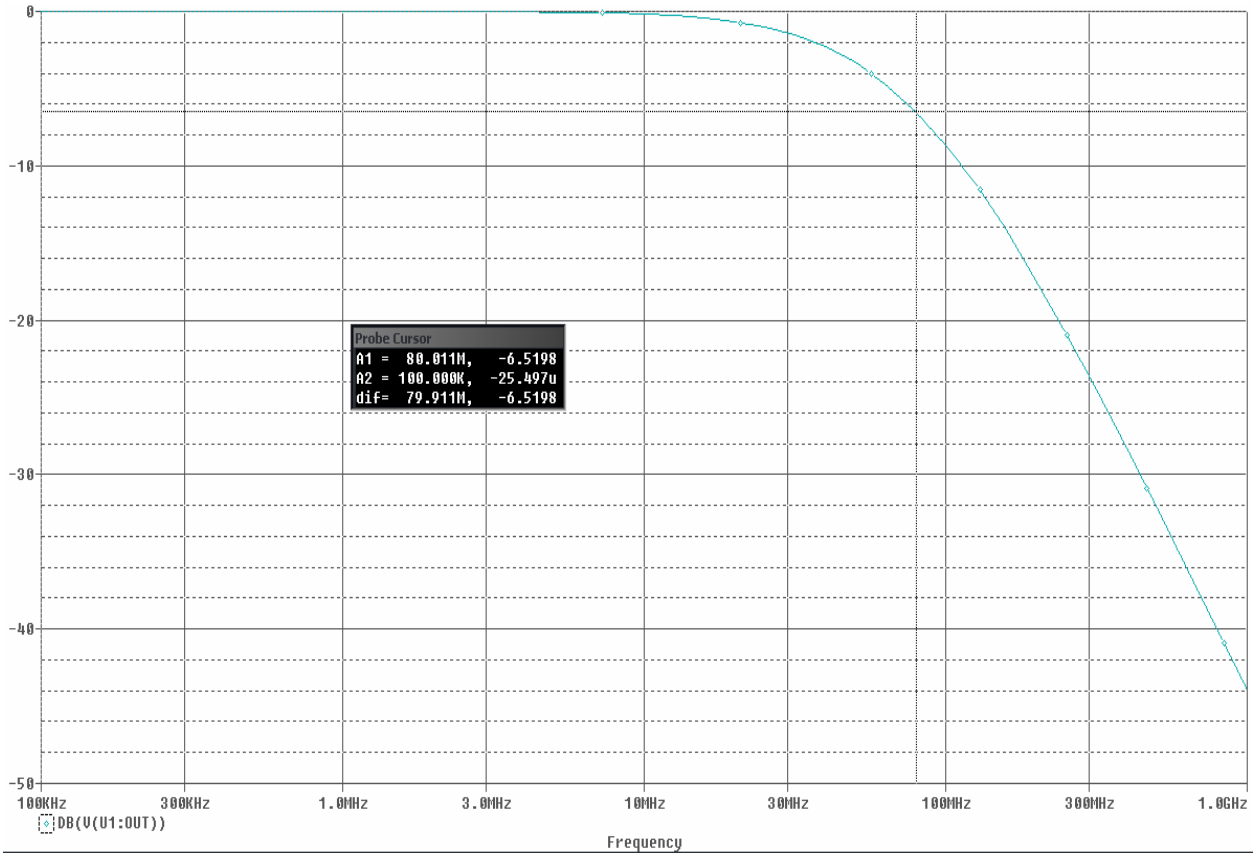

Figure 31 Sallen-Key LPF Vout(dB) vs Frequency—80MHz

4.6 Analog-to-Digital Converters specifications

There are two ADCs on this board. One is of 80MSPS and the other is of 160MSPS. The T and L inputs for each channel will be sampled at 80MSPS using a single 2V(p-p) ADC input using time multiplexing which is equal to sampling at 40MSPS for T and L. The part used for the 80MSPS A-D conversion is a dual 12-bit, 80MSPS A-D converter.

The T and L signals are multiplexed into the 80MSPS ADC using four analog switches. The control signals for the switches are given from the FPGA. In this way, by selecting the signals from the FPGA, we can easily multiplex the T0, T1, L0 and L1 signals into the A-D converter.

The energy signals (E) do not need an analog switch because they use a different ADC from that of the T and L signals.

The energy signals will be sampled at 160MSPS with the intention of deriving coincident timing resolution to within 1nsec at FWHM. Electronic timing resolution will be measured using a constant amplitude pulse generator to produce the ideal signal. The part used for the 160MSPS A-D conversion is a dual 10-bit 160MSPS A-D converter.

The outputs of both the ADCs are fed to the FPGA, where further processing is done.

4.7 Clocking Specifications

The APD algorithm prototype board energy signals are capable of deriving the sample clock from either:

1. An on-board LTC6905 programmable oscillator or
2. An on-board fixed SEL3823B 160MHz crystal.

The 160Msps ADC also can operate at a reduced speed of 100Msps using the synchronous 100MHz clock provided at the digital interface connector.

The T and L signals' ADC sample clock frequency will be derived inside the FPGA using a DLL to derive the 50MHz (100MHz synchronous) or 80MHz(160MHz asynchronous) sampling clock. The effective sample rate at the block T and L signals is 40Msps due to the multiplexing.

5 CONCLUSION AND FUTURE WORK

In this chapter, the conclusions of this thesis and suggestions for future work have been presented.

5.1 Conclusion

This thesis has presented the design and analysis of an Avalanche Photodiode based signal processing board for a Positron Emission Tomography scanner's detector electronics assembly. The design specifications have been met with sufficient margin. PCB signal integrity analysis of critical signals is performed on the proof-of-principle PCB. Results have been verified with Hyperlynx signal integrity tool and critical nets are compared with measured results of the manufactured board.

The analog circuits have been verified to be working satisfactorily.

5.2 Future Work

This board can be used for analysis, development, and derivation of the analog shaping filter and digital processing algorithms required to do a digital implementation of the current front-end analog pole/zero filter. The pole-zero filter is required to reduce

dead-time losses in a charge sensitive preamplifier implementation at high count rates. This board can also be used as a prototype for analysis and testing different new ideas in the direction of improving the performance of the analog subsection.

The timing zero-crossing point and digital timestamp will be integrated into the top-level FPGA project after independent development in the Siemens Medical Molecular Imaging PET Electronics R&D group.

This design is planned to eventually be used with PMT/APD detectors for activity rates up to 1 Mevents second. The advantages of this work would be decreased channel cost and smaller area for a higher level of integration.

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